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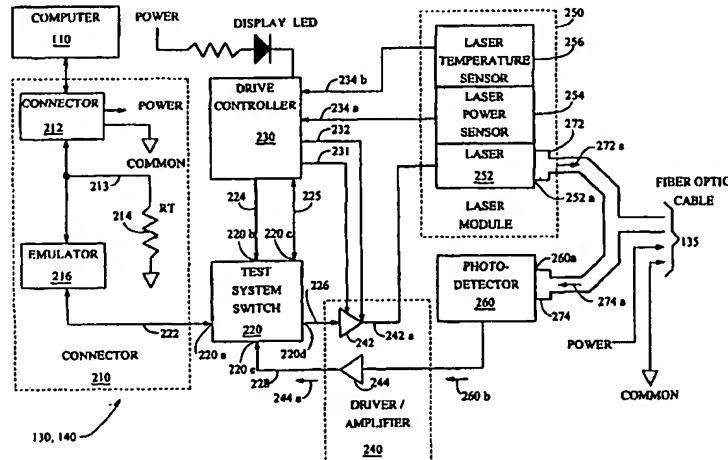
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(54) Title: ELECTRO-OPTIC INTERFACE SYSTEM AND METHOD OF OPERATION



(57) Abstract: An electro-optic interface system (100) configured to communicate, via an optical channel, an electronic signal between a first (110) and a second electronic system (120) includes a first electro-optic transceiver (130), an optical channel and a second electro-optic transceiver (140). The first electro-optic transceiver (130) includes a signal port coupled to the first electronic system (110) and an output coupled to the optical channel and includes a first transceiver emulator circuit (216), and a first transceiver laser (252). The first transceiver emulator circuit is configured to receive an electronic signal (260) comprising parallel data from the first electronic system (110) and, in response, produces serialized data. The first transceiver laser (252) produces a first modulated output signal corresponding to the electronic signal communicated from the first electronic system (110). The first electro-optic transceiver (130) communicates with the laser (250) to determine the operating characteristics and further analyses the returned signal (260b), wherein a processor within the drive controller (230) makes a determination of whether an adjustment in the operating characteristics of the laser (250) would result in improved performance of the optical link. The drive controller (230) dynamically alters the operating characteristics of the laser (250) if the determination is positive. The second electro-optic transceiver (140) includes a first port coupled to the optical channel and a second port.

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coupled to the second electronic system (110). The second transceiver (140) includes a second transceiver photodetector, and a second transceiver emulator circuit. The second transceiver photodetector is configured to receive the first modulated output signal emitted by the first transceiver laser and, in response, produces a first received signal. The second transceiver emulator circuit is configured to receive the received signal comprising serialized data and to produce in response parallel data.

ELECTRO-OPTIC INTERFACE SYSTEM AND METHOD OF OPERATION

BACKGROUND

The present invention relates to an electro-optic communication system and more specifically to an electro-optic interface system configured to optically

5 communicates signals between two or more electronic systems.

Conventionally, electronic systems such as PCs, Internet Servers and Computer Peripherals utilize a variety of metal cables and interface circuits for Interconnection purposes in order to transmit bi-directional information. These interfaces host a variety of communication protocols between the different devices. In many cases, these interfaces 10 limit the performance of the transmission system. Common problems limiting metal cable performance include significant degradation due to problems caused by Radio Frequency Interference (RFI), data transmission speed limitations due to the constrained transmission capability of the cable utilized by standard interfaces (twisted pair, coax cable and other types of interfaces), limited transmission distances for sending data and 15 information due to the limitations of the electronics' transmission system over metal lines.

Fiber optic interface systems have been proposed as a possible solution to many of the aforementioned problems. As a result, fiber optic interface systems have been developed in specific applications for connecting electronic systems such as computers 20 and peripherals. Unfortunately, the existing fiber optic interface systems usually consist of highly complex interface cards, which connect to the back plane of the PC or server host with an adapter card. The adapter card typically includes relatively slow speed electronics needed to drive the fiber optic interface and to establish the necessary protocol to interface with the Host Computer or the Computer Peripheral. As a result, 25 conventionally implemented fiber optic interface systems suffer from limited data rates and bandwidth.

In the past the nature of optical conversion of electronic data signals has been complicated by the need to provide protocol and handshaking communication on either side of the optical converters. Hence although the transfer of data over the majority of the 30 distance between electronic systems is achieved with much greater speed over the optical portion of the link, this transfer speed is reduced significantly by the need to negotiate suitable protocols on either side of the optical connectors. Additionally, complex buffering and timing arrangements were also traditionally required to ensure a seamless

flow of data from one electronic device to the other over the link as a whole.

The electro-optic interface system with which the invention is concerned is ideally suited to USB ver. 2.0 signals which have an alleged data transmission rate of 480Mbps. At this rate, the signal carried on conventional wire cables of any significant length will 5 deteriorate significantly as a result of noise and electromagnetic interference, particularly where such an interface is used to connect a plurality of different peripherals together. Accordingly, to reduce the effect of this it is proposed to reduce the length of any conventional wire or metal conductors as much as possible and provide an optical link over which the signals can be transmitted over the majority of the distance before 10 converting the optical signals back to electrical signals at the location of the peripheral.

It is an object of the present invention to provide an electro-optic interface system which will provide a high speed, high frequency communication link between two or more electronic systems.

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SUMMARY OF THE INVENTION

The present invention provides an electro-optic system and method of operation for communicating high frequency analog and high speed digital signals between two or more electronic systems.

According to a first aspect of the invention there is provided an electro-optic 20 transceiver configured to communicate signals between an electronic system and an optical system comprising a host interface for connecting the transceiver to the electronic system a drive controller, a test system switch (TSS) coupled to both the host interface and the drive controller allowing communication of electronic signals between the host interface 25 and the drive controller and said TSS, said TSS having at least one drive controller signal input and output permitting communication with the drive controller, and a primary signal input and output for receiving signals representative of those received from the optical system and transmitting signals for conversion into optical signals to be transmitted to said optical system respectively, a laser having an input coupled to the 30 primary signal output of the TSS and an optical output coupled to the optical system a photodetector having an optical input coupled to the optical system and an output coupled to the primary signal input of the TSS, said TSS having controllable switch means therein to which the various inputs and outputs of said TSS are connected and

which in a first state permit transfer of electrical signals from the host adapter to the laser for conversion into optical signals and of signals from the photodetector representative of optical signals to the host adapter, characterized in that in said first state said switch means are arranged to deliver the signal received at said primary signal input to both said host adapter and to said drive controller on a drive controller output, said drive controller having analysis means which on recognizing a particular signal received by said TSS on said primary signal input alters the state of said switch means to connect the primary signal input with the primary signal output in a shunt configuration.

Preferably the switch means in said TSS in the first state permit the signal received at the primary signal input to be routed through said TSS to both the analysis means of the drive controller and the host interface and in a second state route said signal directly to an Input/Output module within said drive controller.

Further preferably the drive controller comprises signal generation means and a signal generation means output which is connected to said TSS, said switch means within said TSS being selectively switchable by said drive controller between the first state in which the signal from the host interface is routed through said TSS to the primary signal output thereof and a second state wherein the signal from the host interface is replaced by the signal from the signal generation means.

The nature and advantages of the present invention will be better understood with reference to the following drawings and detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A illustrates a first embodiment of an electro-optic interface system in accordance with the present invention.

Fig. 1B illustrates a second embodiment of an electro-optic interface system in accordance with the present invention.

Fig. 2A illustrates a first embodiment of an electro-optic transceiver in accordance with the present invention.

Fig. 2B illustrates a second embodiment of an electro-optic transceiver in accordance with the present invention.

Fig. 3A illustrates a first embodiment of an emulator circuit in accordance with the present invention.

Fig. 3B illustrates a second embodiment of the emulator circuit in accordance with

the present invention.

Fig. 4 illustrates one embodiment of the test system switch in accordance with one embodiment of the present invention.

5 Figs. 5A and 5B illustrate a flowchart describing the operation of the electro-optic interface system in accordance with one embodiment of the present invention.

Figs. 5C illustrates the signal flow within a representative link during the signal communication process described in Figs. 5A and 5B.

10 Figs. 6A and 6B illustrate a flowchart describing one embodiment of a link characterization performed in accordance with one embodiment of the present invention.

Fig. 6C illustrates the signal flow within a representative link undergoing the link characterization process described in Figs. 6A and 6B.

Figure 7 illustrates the electro-optic interface system as embodied in a universal serial a bus in accordance with one embodiment of the present invention.

15 Fig. 8 illustrates the electro-optic interface system as embodied in a next generation input/output system in accordance with one embodiment of the present invention.

Fig. 9 illustrates the electro-optic interface system as embodied in a logic analyzer system in accordance with one embodiment of the present invention.

20 Fig. 10 illustrates the signal path the test system switch.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

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25 I. Definition of Terms
II. Electro-Optic Interface System Architecture
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IV. Link Characterization
V. Applications

30

I. Definition of Terms

As used herein, the term "laser" refers to a light emitting device, including but not limited to a laser diode or circuit, a light emitting diode (LED), or other optically

transmitting devices. The laser may be formed separately or integrated with other devices or circuitry, for instance a monitoring photodiode, temperature sensing circuitry, or a heating and/or cooling element.

As used herein, the term "electronic system," refers to any device, component or

5 system which processes and or communicates information in electronic form. Possible examples of electronic systems include computers or other electronic processor-controller systems, electronic test equipment, electronic circuitry, electronically based amplifiers, oscillators, filters, transistors, or other components, and electronic portions of electro-optic components such as lasers and photodetectors.

10 As used herein, the term "optical channel" or "optical link" refers to any medium capable of supporting the propagation of a desired wavelength of light. Some examples of an optical channel include a fiber optic cable or other guided medium, a terrestrial or space-based free-space link, or links established in and/or through other mediums such as an aqueous environment through which the desired wavelength of light may be

15 propagated.

II. Electro-Optic Interface System Architecture

Fig. 1A illustrates a first embodiment of an electro-optic (e-o) interface system 100 configured in accordance with the present invention. The e-o interface system 100

20 includes first and second electronic systems 110 and 120 coupled via a fiber optic cable 135 and first and second electro-optic transceivers 130 and 140, respectively. It will be appreciable to those of skill in the art that the invention is not limited to communicating signals between two electronic systems, and that three or more electronic systems may also be connected. Further, the electronic systems 110 and 120 may be an electronic;

25 component, circuit, device or system of any type. Additionally, optical communication may be made through the use of free-space lasers and receiver components as an alternative to the fiber optic cable 135.

Fig 1B illustrates a second embodiment of an electro-optic communication system in accordance with the invention. A description of this embodiment is further provided

30 below.

Fig 2A illustrates a first embodiment of the first and second e-o transceivers 130 and 140 for use with the system shown in Figs. 1A and 1B. The e-o transceiver 130,140 includes a host interface 210, a test system switch 220, a drive controller 230, an

amplifier/driver assembly 240, a laser transmitter 250, a photodetector 260. The laser transmitter 250 and photodetector 260 are coupled to a fiber optic cable 135 via fiber connectors 272 and 274, respectively.

The host interface 210 includes a connector 212, a bus 213, and an emulator circuit 216. The connector 212 is configured to efficiently communicate parallel and/or serial digital data, analog signals, as well as control, power, and other signals between the first electronic system 110 and the e-o transceiver 130.

Depending upon the application, the connector 212 may take a multitude of various forms. For instance, in one embodiment, the connection 212 may be a Universal Serial Bus (USB) connector used to communicate serial data between the electronic systems 110 and 120 comprising a host computer 110 and a peripheral unit 120. In a second embodiment, the connector 212 may be a small computer system interface (SCSI) connector operable to communicate parallel data to and from the first computer 110. Other connector types, such as shielded or unshielded plugs, microwave frequency connectors such as a SMA connector, or specially designed connectors may be used depending upon the type of electronic system 110 generating the data.

Signal communication to and from the computer 110 is provided via a signal bus 213. The signal bus 213 may include one or more serial and/or parallel lines for communicating data, control lines, power lines, and the like. The signal bus 213 may comprise a USB or SCSI bus for communicating serial or parallel data, respectively, to/from a host computer 110. In another embodiment, the signal bus 213 may comprise a general purpose instrument bus (GPIB) used to communicate signals between remotely located electronic test equipment components. In a fourth embodiment, the signal bus 213 includes high frequency transmission lines configured to communicate signals in the HF, VHF, UHF, EHF, RF, microwave, millimeter wave frequency range. As those of skill in the art will appreciate, the present invention is applicable to a wide variety of electronic systems, and accordingly, bus configurations used therewith may be implemented.

One or more terminating resistors 214 may be coupled to the signal line(s) along the signal bus 213 in order to reduce signal reflections occurring therealong. In one embodiment, the terminating resistor(s) has a resistance value which aids to match the output impedance of the computer 110 to the characteristic impedance of the signal line(s). In a specific embodiment, the terminating resistor is substantially 50 ohms, although other values, higher and lower, may be used in alternative embodiments.

The host interface 210 may further include an emulator circuit 216. The emulator circuit 216 operates in a manner that is substantially transparent to the computer or other electronic system and provides substantially real time communication between electronic systems 110 and 120 without reproduction of most or all of the I/O protocol as in the 5 conventional system.

Fig. 2B illustrates a second embodiment of an e-o transceiver 130, 140 configured to operate in a wavelength division multiplexed (WDM) system. This embodiment is further described below.

Fig. 3A illustrates an exemplary embodiment of the emulator circuit 216 in 10 accordance with the present invention. The emulator circuit 216 includes n bus transceivers 302, an nx1 data serializer 306, and 1xn data de-serializer 312.

During data transmission from the computer 110, n-bit parallel data is communicated along the computer bus 213 to the emulator 216. The n bus transceivers 302 are coupled to condition and output the parallel data 304 to the nx1 data serializer 15 306. The nx1 data serializer 306 re-orders the incoming parallel data to produce a serial data stream 308. In one embodiment, the nx1 data serializer 306 includes a system clock and an encoder configured to encode the data with a time stamp to aid in parallel data reconstruction during reception within the second e-o transceiver 140.

During data reception, serialized data 310 transmitted from the peripheral device 20 120 is received from the test system switch 220 and input to the 1xn data deserializer 312. The 1xn data de-serializer 312 performs the inverse function of the data serializer 306, i.e., it restores the incoming serial data to its originally transmitted n-bit parallel form. In the illustrated embodiment, the 1xn data de-serializer 312 includes a data decoder to extract the encoded time stamp of the serialized data to aid in the parallel reconstruction 25 of the data. The restored parallel data 314 is supplied to bus transceivers 302, which conditions and outputs the parallel data to the first computer bus 213. Possible examples of the n x 1 data serializer 306 and 1 x n de-serializer 312 which may be used, include the 16-bit, 2.5 Gbps MAX3880 and MAX3890, available from the Maxim Corporation of Sunnyvale, California. Of course, serializers and de-serializers and de-serializers of other 30 bit capacity, transmission rate, and functionality may be used with the present invention.

The emulator 216 may include additional hardware, software, and/or firmware to enhance operation. A few of the possible additions include local memory buffers, direct memory access (DMA) control, operating system protocol, firmware, and threshold

detectors operable to determine the state of multi-level logic used, for instance, in some forms of USB protocols. Those skilled in the art will appreciate that other hardware, software and/or firmware may be used alternatively, or in addition to that described herein.

5 Fig. 3B illustrates a second embodiment of the emulator 216 configured to operate with a USB 2.0 bus in accordance with the present invention. The emulator 216 is connected to a standard USB transceiver 212 having a high speed current driver 320 configured to drive a differential signal on the USB 2.0 bus 326. The transceiver 212 further includes a high speed differential data receiver 322 configured to receive 10 differential data and convert it to a single-ended mode. The transceiver 212 may further include pull down resistors 324 in conformance with the USB interface specification. The emulator 216 may include pull up resistors R_p coupled to a power supply V_{CC} and switches as dictated by the USB specs. The two differential signal lines as well as power and ground lines are connected to the emulator 216 at the USB interface 328.

15 The emulator 216 includes transmitting circuitry including a differential-to-single-ended receiver 336, a serializer 338, and a buffer 340. The differential-to-single-ended receiver 336 receives the differential signal from the differential bus 334 and converts it to a single ended signal. The serializer 338 operates in the manner described above and may include circuitry to time stamp and encode the processed data to aid in construction 20 during reception at the second e-o transceiver 140. The serializer 338 may further include additional inputs 346 to receive other signals generated and/or received by the emulator 216 for transmission to the second e-o transceiver 140. In addition, the deserializer may further include outputs 352 for supplying additional signals transmitted by the second e-o transceiver 140. A buffer 340 is coupled between the serializer 338 and the test system 25 switch 220 to provide the level shifting, impedance matching, isolation, amplification or other signal conditioning needed to match the serializer output to the test system switch input. Terminating resistors 330 are used to terminate signals.

 The emulator 216 further includes reception circuitry designed to perform the inverse of the emulator's transmitting circuitry. The reception circuitry includes a buffer 346, a de-serializer 348 and a single-ended-to-differential driver 350. The buffer 346 is coupled to the test system switch 220 and provides the signal conditioning necessary to receive the received signal into the de-serializer 348. The de-serializer 348 operates as described above, restoring the incoming serial data to its originally transmitted parallel

form. The de-serializer 348 may include a data decoder to extract the encoded time stamp of the serialized data to aid in the parallel reconstruction of the data. The de-serializer may further include signal outputs 352 configured to provide additional signals transmitted from the emulator or other circuit within the second e-o transceiver 140. The 5 single-ended to differential driver 350 receives the de-serialized data and drives the differential bus 334 in an appropriate manner.

Those of skill in the art will further appreciate that the illustrated embodiments represents only a few of the possible emulator circuits and that other emulator circuits compatible with other bus architectures may be constructed based upon the foregoing 10 description. A variety of different emulator circuits may be constructed to support signal communication between the electronic system 110 and the e-o transceiver 130 consistent with the implemented bus architecture.

Referring again to Fig. 2A, the emulator circuit 216 is coupled to a signal port 220a of the test system switch 220 via an emulator signal line 222. The emulator signal 15 line 222 may consist of a single bi-directional line, or separate signal lines configured to communicate emulator data (e.g., 308 and 310 in Figure 3A) to and from the first computer 110.

The test system switch 220 includes a control input 220b coupled to control line 224 and a second signal port 220c coupled to signal line 225. The drive controller 230 20 controls the state of the test system switch 220 via control line 224. In addition, the drive controller 230 communicates signals to and from the test system switch 220 via signal line 225. The signal line 225 may be used to perform a link characterization, the process of which is further described below. The signal line 225 may consist of a single, bi-directional line or separate signal lines configured to communicate data to and 25 from the test system switch 220. In a further embodiment, control and signal lines 224 and 225 may comprise a bus operable to communicate data, control, ground and/or power signals.

Table 1, shown in Figure 10, illustrates the signal paths which the test system switch 220 connects during transceiver transmission, reception, and link 30 characterization (described below) processes. During signal transmission, the test system switch 220 connects signal port 220a to the first output port 220d, thereby connecting signal line 222 to 226. During signal reception, the test system switch 220 connects the first input port 220e to the signal port 220a, thereby connecting signal line

228 to 222. The test system switch 220 is operable in additional states to perform diagnostic tests locally and on the communication link between e-o transceivers 130 and 140. This process is described in detail in table I, illustrated in Figure 10.

Fig. 4 illustrates one possible embodiment of the test system switch 220 in accordance with one embodiment of the present invention. The test system switch 220 includes (3) single-pole, double-throw switches K1, K2 and K3. The switch K1 has a pole coupled to the signal output line 226, a first throw A coupled to a drive controller/output signal line 225a, and a second throw B coupled to an emulator output signal line 222a. The switch K2 has a pole coupled to the signal input line 228, a first throw A coupled to a drive controller/input signal line 225b, and a second throw B coupled to an emulator signal output line 222b. The switch K3 includes a pole also coupled to the signal input line 228, a first throw A coupled to a drive controller/signal detector input 225c, and a second throw B coupled to the output signal line 226.

During transceiver transmission, switch K1 is controlled via control line 224a to connect emulator output signal line 222a to the signal output line 226. As a result, the signal to be transmitted (serialized data 308 in the illustrated embodiment) is supplied to the laser driver/amplifier 242. During receiver reception, switch K2 is controlled via control line 224b to connect the signal input line 228 to emulator input signal lines 222b. This connection allows the photodetector amplifier output (serialized data 310 in the illustrated embodiment) to be supplied to the emulator 216.

The test system switch 220 also operates in a link characterization mode, further described below. During a link characterization, switch K1 is controlled via control line 224a to couple in the signal generator 431 of the drive controller 230 to the laser driver/amplifier 242. The signal generator 431 provides a reference signal which may be a dc or ac signal, in either analog or digital form. During this operation, switches K2 and K3 are preferably switched to position A.

Within the second e-o transceiver 140 during link characterization, the test system switch 220 is controlled to configure a return shunt path. Specifically, switch K3 is controlled to occupy position A to route the photodetector output 228 to a code detector 435 located within the drive controller 230. The photodetector output 228 has a characteristic such that the code detector 435 will recognize the receipt of such a signal as the initiation of a link characterization. In one embodiment the photodetector output 228 is a predefined binary word. Once received, the code detector 435 subsequently supplies an output to the

drive controller processor 434 informing the processor 434 that a link characterization is underway.

Responsive to the received digital word from the code detector output, the processor 434 instructs the I/O controller 432 to switch (via control line 224c) switch K3 to position 5 B thereby connecting the photodetector amplifier output 228 to the laser driver/amplifier input 226. This configures the shunt return path within the second e-o transceiver 140. The laser driver/amplifier 242 conditions the signal and outputs a driving signal to modulate the laser module 250, thereby providing a returning optical signal to the first e-o transceiver 130. Preferably, the second e-o transceiver I/O controller 432 controls switches K1 and K2 10 to occupy position A.

Within the first e-o transceiver 130, the returned optical signal illuminates the photodetector 260. The photodetector 260 outputs a return reference signal which is further conditioned by the photodetector amplifier 244. The switch K2 is set to position A if not already engaged, thereby routing the returned reference signal at the photodetector output 15 228 to the I/O signal input 225b. As further described below, the drive controller 230 subsequently compares the reference signal output from the signal generator 431 and the returned reference signal received from the photodetector amplifier output 228 to determine the existence and quality of the communication link.

The test system switch 220 is selected to operate with minimal signal loss and 20 distortion over the desired frequency range of interest. An exemplary embodiment of the test system switch includes the series UMI high frequency switches manufactured by the Fujitsu Corporation of Japan.

Referring again to Fig. 2A, the e-o transceiver 130, 140 further includes a drive controller 230 configured to control the operation of the laser transmitter module 250 as 25 well as other operating conditions of the e-o transceivers 130, 140. The construction and operation of the drive controller 230 is further described in the concurrently filed, provisional patent application entitled "Drive Controller and Method of Operation".

Each of the e-o transceivers 130, 140 further includes a driver/amplifier assembly 240. The driver/amplifier 240 includes a laser driver/amplifier 242 and a photodiode 30 amplifier 244. The laser driver/amplifier 242 is used to provide a driving signal 242a to the laser module 250. The laser driver/amplifier has an input signal port coupled to the test system switch 220 via signal line 226, an output signal port, and a control port coupled to the drive controller 230.

In the illustrated embodiment in which the electronic signals are digital serialized data, the laser driver/amplifier 242 is operable to provide sufficient gain/attenuation such that the driving signal 242a corresponding to a "0" or lowest logic level received produces a driving signal which is slightly above the threshold current of the laser 252. In another 5 embodiment in which linear operation is desired and analog signals are provided, the laser driver/amplifier provides sufficient gain and output power such that the driving signal 242a corresponding to the applied linear signal modulates the laser 252 over a substantially linear region of the laser output power response P_{out} vs. $Signal_{in}$.

The laser driver/amplifier 242, may, in one embodiment be a variable gain/output 10 power amplifier in which the gain or output power of the incoming signal is programmable by the direct drive controller 230 via control line 231. The driver amplifier is preferably a high speed/high frequency digital or analog driver circuit capable of handling high speed digital or high frequency analog signals with minimal distortion. For instance, the laser driver/amplifier 242 may be operable to process signals within the LF, MF, HF, VHF, 15 UHF, EHF, microwave, and millimeter wave bands or anywhere therebetween.

In one embodiment, the laser driver/amplifier 242 forms a voltage-controlled current source used to drive the laser module 250. In this embodiment, the laser driver/amplifier 242 may include an operational amplifier such as part number AD8001 20 operational amplifier available from Analog Devices Corporation. The amplifier's output is coupled to the base terminal of a high speed/high frequency transistor, such as part number MMBR941 available from the Motorola Corporation. The amplifier's inverting input is 25 coupled to the emitter terminal of the transistor and an emitter resistor coupled therebetween and ground. The non-inverting input is used as the voltage input to generate the necessary current output at the transistor's collector terminal. The foregoing represents only one of many possible laser driver/amplifier configurations and those of skill in the art will appreciate that others are possible.

The driver amplifier assembly further includes a photodetector amplifier 244. The photodetector amplifier 244 has an input signal port coupled to the output of the photodetector 260 and an output port coupled to the test system switch 220 via signal line 30 228. The photodetector amplifier 244 may further include a control line (not shown) coupled to the drive controller 230 for controlling its operation (e.g., gain and/or output power). The photodetector amplifier 244 is also a high speed digital/high frequency analog

device in its preferred embodiment and able to handle signals within one or more of the aforementioned frequency ranges with a minimal of signal distortion. In one embodiment, the photodetector amplifier 244 consists of the aforementioned operational amplifier AD8001 available from Analog Devices Corporation. Of course, other amplifiers are

5 compatible with the present invention and may be used alternatively.

The e-o transceiver 130, 140 further includes a laser module 250 configured to convert and optically communicate the received data. In one embodiment, the laser module 250 includes a laser 252, a laser power sensor module 254 and a laser temperature sensor module 256. In an alternative embodiment, a heating and/or cooling element (e.g., a Peltier junction) may be included to control the operating temperature of the laser 252 in response to control signals supplied from the drive controller 230.

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The laser 252 includes a signal input configured to receive the driving signal 242a and an optical output for providing a modulated optical output 252a. A variety of laser structures may be used. For instance, the laser 252 may be a homojunction surface or edge-emitting light emitting diode (LED), a single or multiple heterostructure laser diode (LD) or other laser type. Moreover, the laser module 250 may be designed to emit light at a substantially a single mode or wavelength or, alternatively, capable of transmitting light in multiple modes or wavelengths simultaneously, for instance in wavelength division multiplexing (WDM) systems. In case of the latter, the laser 252 may include multiple

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signal inputs for receiving parallel signals, thereby generating a multiple wavelength output corresponding to the parallel signal input.

In addition, if a semiconductor laser is used, a number of different materials may be employed. For instance, SiO_2 , GaP, GaAs, GaAsP, AlGaAs, and InGaAsP, are only a few of the possible materials which may be used. Those skilled in the art will appreciate that the

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present invention is not limited to a laser of a specific type, and that lasers of other architectures and/or semiconductor materials may be used in alternative embodiments.

The power sensor 254 includes a sensor output coupled to sensor line 234a for communicating power monitoring signals relating to the output power of the laser 252. In one embodiment, the laser power sensor includes a monitoring photodiode which is

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optically coupled to the laser 252 and operable to convert the coupled power to an electronic signal for detection by the drive controller via sensor line 324a. Of course, other laser power sensing structures are possible.

The temperature sensor module 256 includes a sensor output coupled to the sensor

line 234b for communicating temperature monitoring signals relating to the operating temperature of the laser 252. In one embodiment, the temperature sensor 256 includes a temperature sensing circuit (not shown) which incorporates a precision temperature sensor such as part number LM45B available from the National Semiconductor Corporation. In response to the temperature varying resistance, the temperature sensing circuit will exhibit changes in its operating point which is detectable by the drive controller 230 via sensor line 234b. Other temperature sensing circuits may be used alternatively.

In one embodiment the laser, power, and/or temperature sensor modules 252, 254 and 256 are monolithically formed and integrated onto a single device using semiconductor processing techniques. The integrated construction facilitates manufacturing and obviates the need for interconnecting lines between the modules 252, 254 and 256. As an example, in one embodiment, a laser module 250 having an integrated laser 252 and power sensor module 254 is the 1305 nm single-mode, InGaAsP laser diode (part number FU-411SDF) available from the Mitsubishi Corporation of Japan. An example of an multi-mode laser having an integrated laser and power sensor module 252 and 254 is the Mitsubishi ML4102A 780 nm AlGaAs laser. Other components are available which integrate the laser, power and/or temperature sensor modules.

In an alternative embodiment, some or all of the components 252, 254, and 256 may be separately formed. For instance, the laser 252 may be separately fabricated (perhaps using a more efficient semiconductor material and/or more precise processing technique) from the power and temperature sensor modules 254 and 256 which may be themselves separately or integrally formed. As appreciable to those skilled in the art, separate fabrication of the laser 252 may provide advantages such as improved laser performance as well as higher yield, lower cost and greater reliability in the construction of the laser module 250.

If separately processed, the laser 252 will include sensor outputs (not shown) coupled to communicate the laser power and operating temperature to sensor modules 254 and 256, respectively. In one embodiment, an optical power splitter is used to couple a portion of the laser output power from the laser 252 to the laser power sensor module 254. In one embodiment, the photodetector 260 is a PIN diode, such as part number 1A358 available from the Mitel Corporation.

Optimum performance and accurate control of the laser 252 is in part obtained through monitoring the output signal power through the laser power sensor 254. As more

completely described in applicant's co-pending patent application "Drive Controller and Method of Operation," the drive controller 230 performs a laser output power calibration sequence in which the controller 230 senses the monitoring photodiode current at one or more operating points of the laser module 250, and develops a transfer characteristic of 5 sensed power to optical output power. In response, the drive controller 230 may adjust the operating point of the laser module 250, the gain/attenuation of the laser amplifier/driver 242, or a combination of both, in order to return the laser 252 into the desired window of operation. Sensed temperature data as well as other operating conditions may also be used.

The e-o transceiver 200, Figure 2A (or 130, 140 in Figure 1A) further includes an 10 photodetector 260 operable to detect the received optical signal 260a and provide a received electronic signal 260b in response. Depending upon the system architecture, the photodetector 260 may be designed to have a relatively narrow spectrum overwhich the received light is converted efficiently. For instance, in systems in which a single wavelength of light is used to communicate between units, a relative narrow photosensitive 15 spectrum is used to reduce background noise and interference. Alternatively, the photodetector 260 may operate over a wider photosensitive spectrum. For instance, the e-o interface 130 may be used in a WDM system in which two or more optical wavelengths are transmitted (either from the same e-o transceiver or from different e-o transceivers). In this instance, the photodetector 260 is designed to exhibit a wide photosensitive spectrum 20 overwhich the received light may be converted into electronic signals.

Further, the photodetector 260 may be realized in a variety of different architectures. For instance, the photodetector 260 may be a reversed biased P-N photodiode, a P-I-N diode, an avalanche photodiode (APD), photosensitive transistors, PIN-FETs, as well as other structures. In addition, the photodetector may be made from a wide variety of 25 semiconducting materials, a few examples being SiO₂, GaP, GaAs, GaAsP, AlGaAs, and InGaAsP. Those skilled in the art will appreciate that other photodetector topologies and semiconducting materials may be used in alternative embodiments. In one embodiment, the photodetector 260 is a PIN diode, such as part number 1A358 available from the Mitel Corporation.

30 Optical connectors 272 and 274 provide a low-loss optical connection to the laser 252 and photodetector 260 from the fiber optic cable135. A beam expander (not shown) may be used to facilitate alignment of the connection. In one embodiment, the optical connectors 272 and 274 are FC-PC connectors, such as part number HPC-S0.1 connectors

available from the Rifocs Corporation. In an alternative embodiment in which a free-space optical link is utilized, optical lenses may alternatively be used to collect the transmitted beam.

Although not shown, an optical coupling device may be used to route the

5 transmitted and received optical signals 272a and 274a. The optical coupling device may consist of a directional optical coupler, an optical circulator, an optical switch, or other optical processing components.

Referring back to Fig. 1A, data is communicated between the first and second e-o transceivers 130 and 140 via a fiber optic cable 135. In one embodiment, the fiber optic

10 cable 135 is a duplex fiber cable having two conductive lines for supplying power and ground voltages. In another embodiment, a single mode fiber cable is used such as the SMC-A1060B cable manufactured by the Spectran Corporation. In a third embodiment, a multi-mode fiber cable is used, such as the 530T-01-100S manufactured by the Chromatic Technologies Corporation.

15 In one embodiment of the invention, the e-o transceiver 130, 140 establishes an e-o link between an electronic system 110 and an optical system (not shown) coupled to the optical channel. The optical system may include optical components such as optical amplifiers, filters, mixers, switches, optical computers, optical processors, or other optically-based devices, circuits and/or systems.

20 Fig. 1B illustrates a second embodiment of the e-o interface system 150. In this embodiment, the first and second transceivers 130 and 140 are differentiated by the laser and photodiode modules 250 and 260, respectively. Specifically, the first e-o transceiver 130 includes a laser 252 which emits light at a first wavelength λ_1 , and a photodetector 260 that detects light at a second wavelength λ_2 . The second e-o transceiver 140 includes

25 complementary wavelength components; a laser 252 which emits light at the second wavelength λ_2 , and a photodetector 260 which detects light at the first wavelength λ_1 .

The e-o interface system 150 communicates data in the forward direction (from the first to the second e-o transceiver) using the first wavelength λ_1 and in the reverse direction using the second wavelength λ_2 . The fiber optic cable 135 may be either a single fiber cable

30 capable of supporting the propagation of optical signals at both wavelengths with minimal loss and dispersion, or alternatively, a dual fiber optical cable having dedicated fibers for propagating each wavelength.

Fig. 2B illustrates a second embodiment of the e-o transceivers 130 and 140. In this

embodiment, the transceivers 130 and 140 are configured to operate in a wavelength division multiplexing (WDM) system.

The first and second e-o transceivers 130 and 140 each include n transceiver slices 280, each slice having a connector 212, an emulator 216, a test system switch 220, a laser 5 driver/amplifier 242 and photodetector amplifier 244, a laser module 250, and a photodetector 260. A single drive controller 230 is coupled to and controls each of the transceiver slices 280 via bus lines 285, wherein each bus line 285_x includes signal, control, ground, power, sensor and other lines, described above for the e-o transceiver of Fig. 2A. Each of the transceiver slices 280 operates as described above to communicate dc or ac 10 signals in digital or analog form between the first and second electronic systems 110 and 120.

The laser module 250_x within each of the transceiver slices 280 is designed to emit light at a unique wavelength. A wavelength combiner 290, such as those manufactured by GCA Fiberoptics Ltd., combines light of different wavelengths to produce an output

15 spectrum along the optical channel, a fiber optic cable 135 in the illustrated embodiment. In this manner, the e-o transceiver 130, 140 can communicate multiple channels of data simultaneously between the first and second electronic systems 110 and 120. Other optical components, such as an optical multiplexer, may be alternatively used to combine the optical outputs.

20

III. Electro-Optic System Operation

Figs. 5A and 5B illustrate a flowchart describing the operation of the electro-optic interface system 100 shown in Figs. 1A and 1B. The method is illustrated for a digital communication system configured to optically communicate data in a half-duplex

25 transmission mode, although those of skill in the art will appreciate that the method may be modified to describe the operation of a digital or analog communication system operable in a simplex or full-duplex transmission modes. Fig. 5C illustrates the signal flow within a representative link during the signal communication process described in Figs. 5A and 5B.

Initially at 510, a link characterization is performed to determine the existence and 30 quality of the communication link between electronic systems 110 and 120. This process is further illustrated in Fig. 6 and described below.

Next at 515 (Figure 5), an electronic signal 560 is communicated from the electronic system 110. This process may be achieved using an USB, SCSI or other bus-type

connector. The electronic signal 560 may be a dc or ac signal, in digital or analog form. In the illustrated embodiment, the electronic signals are parallel digital bits.

Subsequently at 520, the electronic signal 560 is supplied to the first transceiver emulator circuit 216, which encodes the electronic signal, producing an encoded signal 562.

5 In the illustrated embodiment, this encoding process includes the processes of time stamping and serializing the parallel bits.

Next at 522, the encoded signal is supplied to a first transceiver laser driver/amplifier 242₁, which in response produces a driving signal 564. This process is performed by controlling the first transceiver test system switch 220₁ to couple the signal 10 paths 222₁ and 226₁ together.

The first transceiver laser driver/amplifier 242₁ is operable to provide sufficient gain/attenuation such that the driving signal 564 corresponding to a "0" or lowest logic level of the electronic signal 560 produces a driving signal 564 which is slightly above the threshold current of the first transceiver laser 252₁. In another embodiment in which linear 15 operation is desired, the first transceiver laser driver/amplifier 242₁ provides sufficient gain and output power such that the driving signal 564 corresponding to the electronic signal 560 modulates the first transceiver laser 252₁ over a substantially linear region of the laser output power response.

Next at 525, the driving signal 564 is injected into the first transceiver laser 252₁, 20 which in response, produces a modulated optical signal 566. In the illustrated embodiment, the first transceiver laser 252₁ is a single mode laser which is modulated by a driving signal 564 composed of serial bits having a "0" or logic low level set slightly above the laser's threshold point. Accordingly, when a "1" or high state is received in the serial data, the laser is modulated on and emits a burst of light. Alternatively, when a "0" or low state is 25 received, the laser is modulated substantially near its threshold current.

Next at 530, the modulated optical signal 566 is communicated along the optical channel 135 and a received optical signal is provided at the second e-o transceiver 140. In the illustrated embodiment, optical communication is a fiber optic cable which has minimal signal loss and dispersion. In an alternative embodiment, the process may be performed by 30 using a free-space optical link. Additional optical devices such as an optical combiner, coupler, or circulator may be used to facilitate optical communication.

Next at 535, the received optical signal illuminates the second transceiver photodetector 260₂ which, in response, produces a received signal 570. In one embodiment,

the received signal exhibits a modulation characteristic which is substantially identical to the driving signal 564, although some variation will occur due to quality of the communication link. For example, in the illustrated embodiment in which the driving signal 564 is a digital signal, the received signal 570 is substantially a digital signal having 5 the substantially the same waveshape, although the two signals may differ in amplitude and bit value in a few instances. The second transceiver photodetector 260₂ may comprise a single or multimode wavelength detector, in which case the second transceiver photodetector 260₂ will output one or multiple received signals, respectively.

Next at 540, the received signal is supplied to a second transceiver emulator circuit 10 216₂ which decodes the received signal 572 and produces a restored signal 574. In the illustrated embodiment, this process is performed by controlling the second transceiver test system switch 220₂ to couple the signal paths 228₂ and 222₂ together.

15 The decoding process 540 comprises the reverse of 520. In the illustrated embodiment, the decoding process 540 includes reading the aforementioned time-stamps encoded in the encoded signal 562, de-serializing the serial bits based upon the time stamp, and level shifting the de-serialized (parallel) bits to the appropriate level required for the second electronic system 120. Additional signal conditioning (de-emphasis) may be included to compensate for the dispersion effects encountered during signal transmission.

At 550, the restored data (parallel digital bits) 574 is communicated to the 20 peripheral device in parallel form. This process may be achieved using an USB, SCSI, GPIB, or other bus-type connector to facilitate connection between the second e-o transceiver 140 and the electronic system 120.

The foregoing illustrates only one possible embodiment of the method for operating the e-o interface systems described herein and those of skill in the art will appreciate that 25 the method of operation of the disclosed e-o interface systems is not limited to the foregoing method. The e-o interface systems described herein may be operated using modified, altered or equivalents methods to achieve the same results.

IV. Link Characterization

30 Figs. 6A and 6 B illustrate a flowchart describing a link characterization 510 shown in Fig. 5A in accordance with the present invention. The link characterization process 510 enables the user(s) of the electronic systems 110 and 120 to determine if a satisfactory communication link has been established or if an established link remains intact. The link

characterization may be performed prior to communicating data between electronic systems and/or periodically thereafter to ensure link satisfactory operation. Fig. 6C illustrates the signal flow within a representative link undergoing the link characterization process described in Figs. 6A and 6B.

5 Initially at 602, a reference signal 650 is supplied to the first transceiver laser driver/amplifier 242₁ in the e-o first transceiver 130. In the illustrated embodiment, this process is performed by controlling the test system switch 220₁ to connect the signal line 225₁ to the input of the laser driver/amplifier 242₁ and supplying a reference ac or dc signal from the first transceiver drive controller 230₁. As further described in applicant's

10 concurrently filed provisional patent application entitled "Drive Controller and Method of Operation," the first transceiver drive controller 230₁ includes a signal generator which produces a reference signal 650 for the link characterization process. In an alternative embodiment, the reference signal 650 is supplied to the input of the first transceiver laser 252₁ directly. Further alternatively, multiple reference signals may be provided by the drive

15 controller 230₁ to provide a multi-wavelength test signal using the e-o transceiver 130, 140 described in Fig. 2B.

Next at 604, the reference signal 650 is conditioned, thereby producing a reference drive signal 652. This step is executed in the illustrated embodiment by level-shifting the serial bits, such that the reference drive signal 652 corresponding to a "0" or lowest logic

20 level is slightly above the threshold current of the laser 252. In another embodiment in which a linear link characterization is desired, the laser driver/amplifier 242₁ provides sufficient gain and output power such that the reference drive signal 652 corresponding to the reference signal 650 modulates the laser 252₁ over a substantially linear region of the laser output power response. As described above, this step may be omitted if the reference

25 drive signal(s) 652 is provided directly to the laser 252₁.

At 606, the reference drive signal 652 is provided to the first transceiver laser 252₁ which, in response, produces a reference optical signal 654. A single mode or multimode laser may be used to generate the reference optical signal 654 responsive to the supplied reference signal or signals, respectively.

30 At 608, the reference optical signal 654 is communicated over the optical link. In the illustrated embodiment, the process is performed by communicating the reference optical signal over a fiber optic cable to provide a received optical signal at the second e-o transceiver 140. The received optical signal 656 is differentiated from the reference optical

signal 654 by connector and signal losses and dispersion due to the bandwidth limitations of the fiber cable. In an alternative embodiment, this process may be performed by using a free-space optical link.

At 610, the received optical signal 656 illuminates the second transceiver

5 photodetector 260₂, which, in response provides a received signal 658. In the illustrated embodiment this process is achieved by employing a PIN diode photodetector. In alternative embodiments, other photodetector structures may be used.

At 612, the received signal 658 is conditioned by the second transceiver photodetector amplifier 244₂, to produce a returning signal 660. This process may include

10 level-shifting, amplification, attenuation, filtering and/or other electronic processing of the received signal.

At 614, a shunt return path within the second e-o transceiver 140 is configured. In the illustrated embodiment, this process is performed by commanding the second transceiver drive controller 230₂, to set the second transceiver test system switch 220₂,

15 therein to connect the output of the photodetector amplifier 260₂ to the input of the second transceiver laser driver/amplifier 242₂. In an alternative embodiment, the return path is configured by connecting the photodetector output to the laser input without routing the returning signal 660 through the photodetector amplifier 244₂, and/or the laser driver/amplifier 242₂.

20 At 616, the returning signal 660 is conditioned by the laser driver/amplifier 242₂, to produce a return drive signal 662. In the illustrated embodiment, this process is performed by controlling the laser driver amplifier 242₂, to impart substantially the same gain, attenuation, filtering, and/or other signal processes to the returning electronic signal 662 as would be imparted to an electronic signal originating from the test system switch 220₂, so

25 that the link may be accurately accessed. This process may be omitted if the photodetector output is coupled to the laser input during the link characterization process.

At 618, the return drive signal 662 is supplied to the second transceiver laser 252₂, which, in response generates a returning optical signal 664. This process is achieved in the illustrated embodiment through the use of a single mode laser, although a multimode laser

30 may be used for the link characterization as well.

At 620, the returning optical signal 664 is communicated over the optical link to produce a returned optical signal 666 at the first e-o transceiver 130. Compared to the returning optical signal 664, the returned optical signal 666 will exhibit signal and/or

waveform degradation due to connector and signal losses and dispersion due to the bandwidth limitation of the fiber cable 135. In an alternative embodiment, this process may be performed by using a free-space optical link.

At 622, the returned optical signal 666 illuminates the first transceiver photodetector 5 260₁, which, in response outputs a returning reference signal 668. In the illustrated embodiment, this process is achieved by employing a PIN diode photodetector. In alternative embodiments, other photodetector structures may be used.

At 624, the returning reference signal 668 is conditioned by the first transceiver photodetector amplifier 244₁, and in response outputs a returned reference signal 670. In the 10 illustrated embodiment, this process is performed by amplifying the returned reference signal.

At 626, a shunt path within the first e-o transceiver 130 is configured to receive the returned reference signal 670. In the illustrated embodiment, this process is performed by controlling the first transceiver test system switch 220₁, to connect the photodetector output 15 228₁ to the drive controller signal line 225₁. As further described in applicant's co-pending patent application entitled "Drive Controller and Method of Operation," the drive controller 230₁, includes a signal receiver for detecting and analyzing the returned reference signal 670. In an alternative embodiment, the first e-o transceiver shunt return path is configured by connecting the output of the photodetector 260 to the digital driver controller signal line 20 225₁.

At 628, the first transceiver drive controller 230₁ compares the reference signal 650 with the returned reference signal 670 to determine the existence and quality of the link between the first and second transceivers 130 and 140. This process may be performed in one embodiment by comparing the reference signal with the returned reference signal. In so 25 doing, a variety of link parameters such as the signal-to-noise (SNR) ratio, bit error rate (BER), effective signal loss, effective channel noise, channel bandwidth, as well as other parameters may be computed. The process of 628 may also include repeating the processes of 602-626 using different reference signals. In this manner, link performance can be accurately simulated under different operating conditions.

30 Next at 630, a determination is made as to whether one, a predefined group or all of the computed link parameters are within the desired window. For purposes of the present invention, "the desired window" may be defined as (1) occurring within a predefined range, (2) exceeding a minimum quantity (such as a minimum SNR requirement), and/or (3) not

exceeding a maximum quantity (such as a maximum NF or BER requirement). If the parameter(s) are determined to be within the desired window, the drive controller 240 sends a signal to the LED 231 to illuminate green, thereby indicating that a satisfactory link with the second e-o transceiver 140 has been established or continues (process 632). The drive

5 controller may communicate a signal to the second e-o transceiver 140 via the aforementioned means to indicate that the link is satisfactory. The second e-o transceiver drive controller may subsequently send a signal to the LED indicator therein to illuminate green indicating a satisfactory link has been established or continues (process 634). Next at 636, the drive controllers communicate their status to their respective systems 110 and 120.

10 In an alternative embodiment in which the e-o interface system is implemented in a USB embodiment, this process is omitted.

If at 630, a determination is made that one, a selected group, or all of the computed link parameters are not within the desired window, the drive controller 240 sends a signal to the LED indicator 231 to illuminate red to alert the user that the link has not been established or that the link has been interrupted (process 638). The drive controller may communicate a signal to the second e-o transceiver 140 via the aforementioned means to indicate that the attempted link is unsatisfactory or has been interrupted. The drive controller in the second e-o transceiver may subsequently send a signal to the LED indicator therein to illuminate red indicating that the link has not been established or

15 interrupted. (process 640). Alternatively or in addition, the electronic systems may include monitoring devices such as a display, printer, or other output devices configured to communicate to the user and/or system maintainer, the computed link performance between the electronic systems 110 and 120. While the computed link performance may not meet a predefined parameter such as SNR or BER, the user(s) may not require such a high quality

20 link and proceed or continue with data transmission.

The drive controller within the first and/or second e-o transceivers may be operable to attempt to diagnose and/or improve the link performance by varying one or more of the operating conditions of the components under its control in light of sensed system performance. For instance, if high signal loss is sensed and the drive controller in the first e-

25 o transceiver detects lower than optimum output power, the drive controller within the first e-o transceiver 130 may be programmed to begin to increment signal gain corresponding to the respective laser driver/amplifier 242 until optimum laser output is achieved and the minimum link parameter is attained. Of course, other scenarios are possible in which the

system is intelligently able to diagnose and correct for link degradation.

If the drive controller(s) are operable to adjust the operating conditions of their respective e-o transceivers, a determination is made at 642 as to whether the conditions are such that an adjustment may improve the link performance. As described above, this 5 determination may be assessed based upon various factors including the sensed transmitted and/or received power, operating conditions, such as temperature, power dissipation, drive signal level, received signal level, computed link parameters or the like. The drive controller(s) may be programmed to adjust any of the operating conditions within its control based upon one or more of these factors. Further, the number of attempts to improve 10 the link may be used as a factor in deciding whether adjustment is possible. For instance, there may be a point at which little or no link improvement is realized. In this instance, the drive controller(s) may be programmed to attempt no further adjustment.

If, given the operating conditions, the drive controller(s) determine(s) that it is possible to improve the link performance, an adjustment is attempted (process 644). As 15 described above, the adjustment may be made at one or both e-o transceivers, for one or more of the operating parameters under the control of the respective drive controller. After that adjustment, the process returns to 630, at which point the aforementioned link parameter(s) are recomputed to determine if an improvement was realized. In one embodiment, only the link parameter(s) which were outside of the desired window are 20 recomputed in order to expedite link repair.

If at 642, a determination is made that link improvement is not possible, the process continues at 646 where the drive controllers inform their respective electronic systems 110 and 120 of the link failure.

In addition to the aforementioned processes, the link characterization 510 may 25 further include configuring the test system switch 220 to connect the emulator line 222 to the drive controller signal line 225 so as to monitor the signal output from the emulator 216. This process provides a local diagnostic capability from the electronic system 110 to the transceiver 130 (and correspondingly from the second electronic system 120 to the second e-o transceiver 150). Thus the local and link diagnostic capabilities collectively 30 provide a diagnostic capability over the entire link from the first electronic system 110 to the second electronic system 120.

The methods of Figs. 5 and 6 may be implemented in a multitude of different forms (i.e. software, hardware, or a combination of both). In one embodiment, the described

methods may be implemented as a software program executed within the processor of the drive controller to control the respective e-o transceivers 130, 140. This process is further described in applicant's concurrently filed provisional patent application "Drive Controller and Method of Operation."

5

V. Applications

The e-o interface systems 100 and 150 of Figs. 1A and 1B, respectively, may be implemented in a variety of different applications to optically communicate data between two or more electronic systems. The following examples are present as only a few of the 10 possible applications of the systems and methods described herein. Those of skill in the art will appreciate that numerous other applications may benefit from the e-o interface system described herein.

Figure 7 illustrates the e-o interface system as embodied in a universal serial bus (USB) configured to communicate signals between a host system 110 and a peripheral 15 device 120. The USB bus can be constructed to provide varying of degrees of speed, bandwidth and link quality. For instance, the USB bus is configured to provide a moderate speed communication link using inexpensive laser diodes, multi-mode optical fibers and inexpensive optical fiber connectors as well as inexpensive computer interface emulators. In an alternative embodiment, a higher speed link may be constructed using single mode 20 lasers and higher quality fiber optic cable and other components.

A duplex fiber optic cable 700 is connected to first and second e-o transceivers 130 and 140 which are encased in connector housings 709 and 711, respectively. A host USB connector 708 and a peripheral USB connector 712 extend from connector housings 709 and 711, respectively, to engage corresponding USB connectors 702 and 718 located on the 25 computer 110 and the peripheral device 120, also respectively. As illustrated, the computer and peripheral device connectors 708 and 712 may be of different sizes to ensure proper connection.

Each of the connector housings 709 and 711 may include one or more LED indicator lights 707 and 715 operable to provide a visual indication of one or more aspects 30 of the system. For instance, the LEDs 707 and 715 may illuminate green when a link of suitable transmission quality has been established between the computer 110 and peripheral device 120. Alternatively, the same or another LED may illuminate red when a suitable link has not been established. In alternative embodiments, some or all portions of the e-o

transceivers 130 and 140 may be fabricated within the line of the computer bus line, within the connector, within the computer 110, or located on a device card installed in the computer 110 and/or in the peripheral device.

Fig. 8 illustrates the e-o interface system as embodied in a next generation

5 input/output (NGIO) system 800 in which a computer server 850 is coupled to a host channel adapter (HCA) 860. The HCA 860 is coupled to a bank of switching networks (an NGIO switch) 870 which contains the hardware and protocols necessary to fan out the communication to one or more devices. Each output of the NGIO switch 870 is coupled to a target channel adapter (TCA) 880, which in turn, provides connectivity to a variety of

10 different components and networks such as to peripheral devices, a local area network or the Internet 890.

The NGIO system 800 is similar to the network architecture employed in a mainframe computer system in which the server computer, memory, and memory management are included within one computer system and the peripheral devices are

15 included within a second computer system. The architecture (referred to as an I/O channel) frees the server computer from management of computer peripherals and communications which tends to slow down the server computer. It is contemplated that the NGIO architecture will be adopted in a variety of applications including providing connectivity to the Internet where the computer server 850 operates as a web server to which one or more

20 of the I/O controllers 890 includes an internet link. In this embodiment, the e-o interface system of the present invention may be established between a variety of points, including between a TCA 880 and an I/O controller 890 and configured in a manner similar to that shown in Fig. 1A.

Fig. 9 illustrates the e-o interface system as embodied in a logic analyzer isolator

25 900 useful for testing a logic circuit 962, such as a microprocessor. The isolator 900 includes a first e-o transceiver 920 having one or more logic probes 922, a fiber optic cable 935, a second e-o transceiver 940, a bus line 942 and a logic analyzer 950. A logic circuit 962 under test may be located on a motherboard 960. A development system 910 couples to the motherboard 960 via a bus line 916 and is used to develop and test the circuit's

30 firmware and operation. Preferably, the fiber optic cable 935 electrically isolates the first e-o transceiver 920 from the second e-o transceiver and does not include an electrically conductive line, such as a power or ground line there between. Electronic isolation between the first and second transceivers 920 and 940 may be accomplished through the use of

battery-powered supplies 925 and 945, or alternatively, through separate ac or dc power supplies.

During operation, one or more parallel logic probes 922 are coupled to the logic circuit 962. The logic probes 922 detect the states occurring along the probed point, each 5 probe typically defining a parallel channel which may be displayed on the logic analyzer display 952. The probes are coupled to an emulator located within the first e-o transceiver 920 which converts the parallel channels of the probed data into a serialized data stream. The serialized data may be encoded with a time stamp as described above to aid in the parallel reconstruction of the data in the second e-o transceiver 940. Within the first e-o 10 transceiver 920, the serialized data is conditioned and injected into the laser transmitter module which, in response, provides a modulated light output along the fiber optic cable. The photodetector within the second e-o transceiver 940 receives the modulated light signal and outputs a received electronic signal representing the transmitted serialized data. The received electronic signal is conditioned, de-serialized, and presented to the parallel 15 detector ports 951 of the logic analyzer via bus line 942. The logic analyzer 950 senses the signals at the detector ports 951 and displays the detected states for each probe channel on the display 952. One or more probe channels may be displayed simultaneously. The data from one or more probe channels may be mathematically combined to display, for instance a sum or difference of two probe channels.

20 Implementation of the e-o interface system with the logic analyzer improves the electronic isolation between the logic analyzer and the logic circuit under test 962. Specifically noise sources 912 and 964 attributable the development tool and system ground noise from other devices will conduct noise currents 971 and 972 to ground via ground terminals 914 and 965. Because the logic analyzer 950 is also connected to ground 25 via terminal 955, the noise currents 971 and 972 may propagate to the logic circuit under test 962 if the communication path 935 was electrically conductive. However, because the communication path is optical and the first and second transceivers 920 and 940 are electrically isolated, the ground currents 971 and 972 are not provided a return path via the logical circuit under test 962. In this manner, development and evaluation of the logic 30 circuit can be performed more accurately.

In an alternative embodiment, the first e-o transceiver 920 consists of an e-o transmitter operable to transmit data and the second e-o transceiver 940 consists of an e-o receiver operable to receive data. In this embodiment, the e-o transmitter 920 is the above-

described e-o transceiver 130 without the associated reception circuitry. For instance, the photodector 260, the photodetector amplifier 244 may be excluded and the bi-directional signal lines may modified as unidirectional signal lines for propagating signal in a single direction. Further, the e-o transmitter emulator may be constructed without the de-serializer or associated circuitry. Other modifications of an e-o transceiver to operate as an e-o transmitter will be apparent to those skilled in the art.

The e-o receiver 940 is similarly modified to include only the reception components and circuitry. For example, the laser driver/amplifier 242 and the laser module 250 may be excluded. Further, the e-o receiver emulator may be constructed without the serializer or associated circuitry. Other modifications of an e-o transceiver to operate as an e-o receiver will be apparent to those skilled in the art.

WHAT IS CLAIMED IS

1. An electro-optic transceiver configured to communicate signals between an electronic system and an optical system comprising:
 - 5 a host interface for connecting the transceiver to the electronic system
 - a drive controller
 - a test system switch (TSS) coupled to both the host interface and the drive controller allowing communication of electronic signals between the host interface and the drive controller and said TSS,
 - 10 said TSS having at least one drive controller signal input and output permitting communication with the drive controller, and a primary signal input and output for receiving signals representative of those received from the optical system and transmitting signals for conversion into optical signals to be transmitted to said optical system respectively,
 - 15 a laser having an input coupled to the primary signal output of the TSS and an optical output coupled to the optical system
 - a photodetector having an optical input coupled to the optical system and an output coupled to the primary signal input of the TSS,
 - 20 said TSS having controllable switch means therein to which the various inputs and outputs of said TSS are connected and which in a first state permit transfer of electrical signals from the host adapter to the laser for conversion into optical signals and of signals from the photodetector representative of optical signals to the host adapter, characterized in that in said first state said switch means are arranged to deliver the signal received at said primary signal input to both said host adapter and to said drive controller
 - 25 on a drive controller output, said drive controller having analysis means which on recognizing a particular signal received by said TSS on said primary signal input alters the state of said switch means to connect the primary signal input with the primary signal output in a shunt configuration.
- 30 2. An electro-optic transceiver according to claim 1 characterised in that the switch means in said TSS in the first state permit the signal received at the primary signal input to be routed through said TSS to both the analysis means of the drive controller and the host interface and in a second state route said signal directly to an Input/Output module

within said drive controller.

3. An electro-optic transceiver according to either claim 1 or 2 characterised in that the drive controller comprises signal generation means and a signal generation means 5 output which is connected to said TSS, said switch means within said TSS being selectively switchable by said drive controller between the first state in which the signal from the host interface is routed through said TSS to the primary signal output thereof and a second state wherein the signal from the host interface is replaced by the signal from the signal generation means.

10

4. An electro-optic system according any preceding claim 1 characterised in that the coupling between the TSS and the host interface is achieved by the connection of a host interface input and output provided on said TSS to an output and input provided on said host interface.

15

5. An electro-optic transceiver according any preceding claim characterised in that the host interface comprises an emulator having an input coupled to receive an electronic signal from the electronic system and an output coupled to the TSS.

20

6. An electro-optic transceiver according to claim 5 characterised in that the emulator comprises a data serialiser configured to receive parallel data from the electronic system and deliver serial data on said output of said host interface and a data de-serialiser configured to receive serial data on said input of said host interface and output parallel data to said electronic system.

25

7. An electro-optic transceiver according to any of the preceding claims characterised in that the lowest logic level of the signal delivered to said laser input emanating from the primary signal output of said TSS is above the threshold current level of the laser.

30

8. An electro-optic transceiver according to any of the preceding claims characterised in that the laser is configured to receive the driving signal and in response output a modulated optical signal.

9. An electro-optic transceiver according to any preceding claim characterised in that a laser driver/amplifier is provided having an input coupled to the primary signal output of the TSS and an output coupled to the input of the laser, the laser driver/amplifier configured to receive a signal from said TSS and in response provide a drive signal.

5

10. An electro-optic transceiver according to claim 9 characterised in that the output level of the drive signal corresponding to the electronic signal modulates the laser over a substantially linear portion of the laser output power response.

10 11. An electro-optic transceiver according to claims 9 or 10 characterised in that a power sensor is provided having an input coupled to the laser and a sensor output coupled to the laser driver/amplifier, the laser power sensor configured to sense the output power of the laser and to produce in response a monitoring signal for controlling the laser driver/amplifier.

15

12. An electro-optic transceiver according to claim 9 or any claim dependent thereon characterised in that a temperature sensor is further provided having an input coupled to the laser and a sensor output coupled to the laser driver/amplifier, the laser power sensor configured to sense the operating temperature of the laser and to produce in response a monitoring signal for controlling the laser driver/amplifier.

20

13. An electro-optic transceiver according to any preceding claim characterised in that two or more TSSs are provided coupled to a corresponding number of host interfaces in turn connected to a plurality of electronic systems, said two or more TSSs configured both 25 to deliver signals on their primary signal outputs to a corresponding number of lasers having optical outputs and receive signals on their primary signal inputs from a corresponding number of photodetectors having optical inputs, said lasers transmitting optical signals over the optical system at a plurality of different wavelengths and said photodetectors configured to receive optical signals at those wavelengths.

30

14. An electro-optic interface system configured to communicate, via an optical channel, a signal between a first and a second electronic system, the system comprising first and second electro-optic transceivers according to any of the preceding

claims coupled to one another over the optical channel, said first electro-optic transceiver being coupled to the first electronic system and said second electro-optic transceiver being coupled to the second electronic system.

5 15. An electro-optic interface system according to claim 14 characterised in that the first electro-optical transceiver laser produces a first optical signal at a first wavelength and the second transceiver laser produces a second optical signal at a second wavelength, the photodetector of said first electro-optical transceiver having an input which is photosensitive at the second wavelength and the photodetector of the second electro-optical transceiver having an input which is photosensitive at the first wavelength.

10 16. An electro-optic interface system of claim 14, wherein the first electronic system comprises a host system comprising a host socket and the second electronic system comprises a peripheral system comprising a peripheral socket, the interface system further comprising:
15 a host connector having a first port configured to engage the host socket on the host system and a second port coupled to the first electro-optic transceiver; and a peripheral connector having a first port coupled to the second electro-optical transceiver and a second port configured to engage a socket located on a peripheral system.

20 17. The electro-optic interface system of claim 14, wherein the first electronic system comprises a target channel adapter having an output coupled to the signal port of the first electro-optic transceiver and the second electronic system comprises an I/O controller having an input coupled to the second port of the second electro-optic transceiver.

25 18. The electro-optic interface system of claim 14, wherein the first electronic system comprises a logic probe having an output coupled to the signal port of the first electro-optic transceiver and the second electronic system comprises a logic analyzer having a detector port coupled to the second port of the second electro-optic transceiver.

30 19. A method for performing a link characterisation between a first electro-optic transceiver coupled to a second electro-optic transceiver via an optical channel in an electro-optic interface system, the method comprising the steps of:

modulating a laser using a reference signal within the first electro-optic transceiver to produce a reference optical signal;

communicating the reference optical signal over an optical channel to the second electro-optic transceiver;

5 illuminating a photodetector within the second electro-optic transceiver with a received optical signal corresponding to the reference optical signal to produce a received reference signal;

modulating a laser using the received reference signal within the second electro-optic transceiver to produce a returning reference signal;

10 illuminating a photodetector within the first electro-optic transceiver with a returned optical signal corresponding to the returning optical signal to produce a returned reference signal and

comparing the returned reference signal with the reference signal.

15 20. A method according to claim 19 wherein the first and second electro-optic transceivers are provided with drive controllers and test system switches (TSSs) having a plurality of switches therein capable of adopting at least a first state and a second state between which they can be switched by said drive controller, said drive controllers having therein reference signal generator means and comparator means.

20

21. A method according to claim 20 characterised in that during a link characterisation the switches in the TSS of the first electro-optic transceiver are configured to deliver the reference signal through the TSS for transmission over the optical channel and to route the returned reference signal to the comparator means in the drive controller for comparison

25 with the reference signal generated therein, and the switches in the TSS of the second electro-optic transceiver are configured to shunt the reference signal received over the optical channel back over said optical channel to the first electro-optic transceiver.

22. A method according to claim 20 characterised in that the drive controller of the

30 first electro-optic transceiver communicates with the laser therein to determine its operating characteristics and further analyses the returned signal received through the TSS of said first electro-optic transceiver, processor means within said drive controller making a determination whether an adjustment in the operating characteristics of the laser would

result in improve performance of the optical link, said drive controller dynamically altering the operating characteristics of said laser if the determination is positive.

23. A method for switching the operation of an electro-optic interface system for

5 communication of signals between a first electronic system and a second electronic system, said interface system comprising a first electro-optic transceiver coupled to the first electronic system and a second electro-optical transceiver coupled to the second electronic system, said first and second electro-optical transceivers being coupled over an optical channel,

10 said interface in a first operative mode allowing transmission of signals between said first and second electronic systems and in a second operative mode performing a characterisation of the quality of the link between the first electro-optic transceiver and the second electro-optic transceiver,

15 said first and second electro-optical transceivers having test signal switches (TSSs) through which signals received from the first and second electronic systems are passed in the first operative mode,

20 characterised in that the TSSs are coupled to drive controllers which monitor the signals received by said TSSs and on identifying a particular signal received by said TSSs switchingly reroute signals so received to the outputs of said TSS.

24. An emulator for use in an electro-optic interface system comprising first and second electro-optic transceivers coupled over an optical channel, said emulator comprising a channel connection through which communication via a plurality of data signals can be achieved with an electronic system and a primary input and output by

25 which serial data signals are received from and on which serial data signals are transmitted to said electro-optical transceivers, said emulator further comprising data serialisation means for converting the plurality of data signals communicated to said emulator through the channel connection into serialised data signals and data de-serialisation means for performing the reverse operation on serial data signals received by

30 said emulator on said primary input to convert same to a plurality of data signal for transmission to said electronic system through said channel connection, characterised in that said data serialisation and de-serialisation means include system clocks operative at a greater frequency than the bit rate of the plurality of data signals received from said

channel connection, said data serialisation and de-serialisation means including an encoder and a decoder respectively for encoding the resulting serialised data signals with a time stamp or for enabling the decoding of received serialised data and conversion thereof into a plurality of data signals at bit rate at which such are received.

5

25. An emulator according to claim 24 characterised in that a the plurality of data signals received through said channel connection are delivered to one or more differential-to-single-ended signal receivers prior to serialisation to enable said emulator to receive differential signals and also in that the plurality of signals resulting from the outputs of the 10 de-serialiser are delivered through a single-ended-to-differential driver for conversion to differential signals prior to being communicated to the electronic system through the channel connection.
26. An emulator according to claim 25 characterised in that the channel connection is 15 a Universal Serial Bus version connector.

AMENDED CLAIMS

[received by the International Bureau on 4 May 2001 (04.05.01);
original claim 19 amended; remaining claims unchanged (2 pages)]

17. The electro-optic interface system of claim 14,
wherein the first electronic system comprises a target
channel adapter having an output coupled to the signal
5 port of the first electro-optic transceiver and the second
electronic system comprises an I/O controller having an
input coupled to the second port of the second electro-
optic transceiver.

10

18. The electro-optic interface system of claim 14,
wherein the first electronic system comprises a logic
probe having an output coupled to the signal port of the
first electro-optic transceiver and the second electronic
system comprises a logic analyzer having a detector port
15 coupled to the second port of the second electro-optic
transceiver.

19. (Amended) A method for performing a link
20 characterisation between a first electro-optic transceiver
coupled to a second electro-optic transceiver via an
optical channel in a electro-optic interface system, the
method comprising the steps of:
25 modulating a laser using a reference signal within the
first electro-optic transceiver to produce a reference
optical signal;

30

AMENDED SHEET (ARTICLE 19)

communicating the reference optical signal over an optical channel to the second electro-optic transceiver;

5 illuminating a photodetector within the second electro-optic transceiver with a received optical signal corresponding to the reference optical signal to produce a received reference signal;

10 modulating a laser using the received reference signal within the second electro-optic transceiver to produce a returning reference signal;

15 illuminating a photodetector within the first electro-optic transceiver with a returned optical signal corresponding to the returning optical signal to produce a returned reference signal;

comparing the returned reference signal with the reference signal; and

20 performing automatic adjustments to the reference laser signal within the first electro-optic transceiver with the use of a drive controller.

20. A method according to claim 19 wherein the first and second electro-optic transceivers are provided with drive controllers and test system switches (TSSs) having a plurality of switches therein capable of adopting at least a first state and a second state between which they can be switched by said drive controller, said drive controllers

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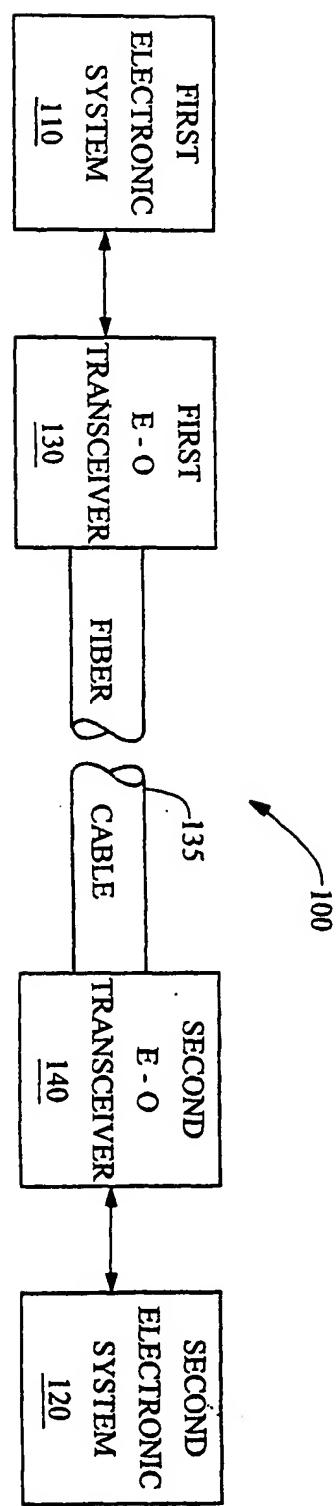


Fig. 1A

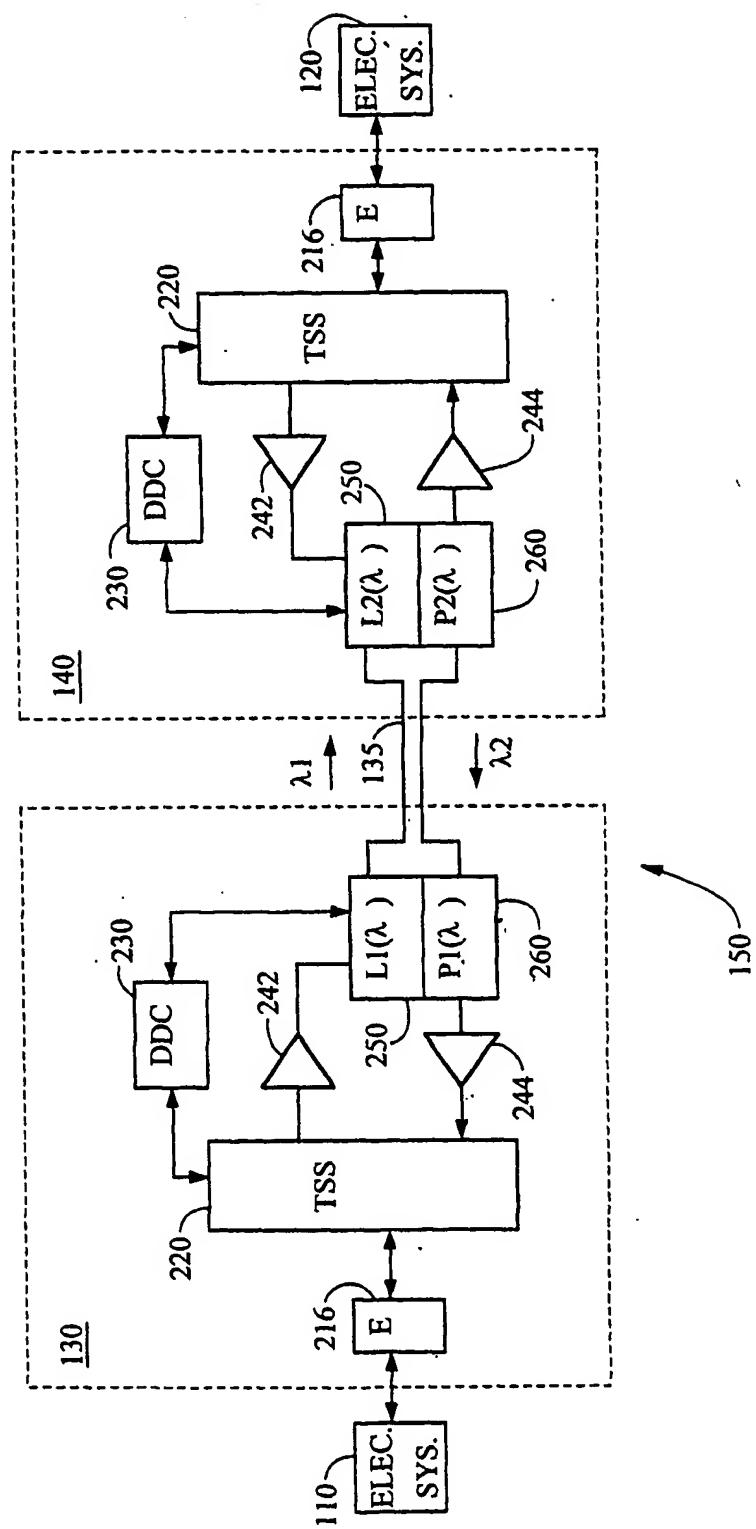
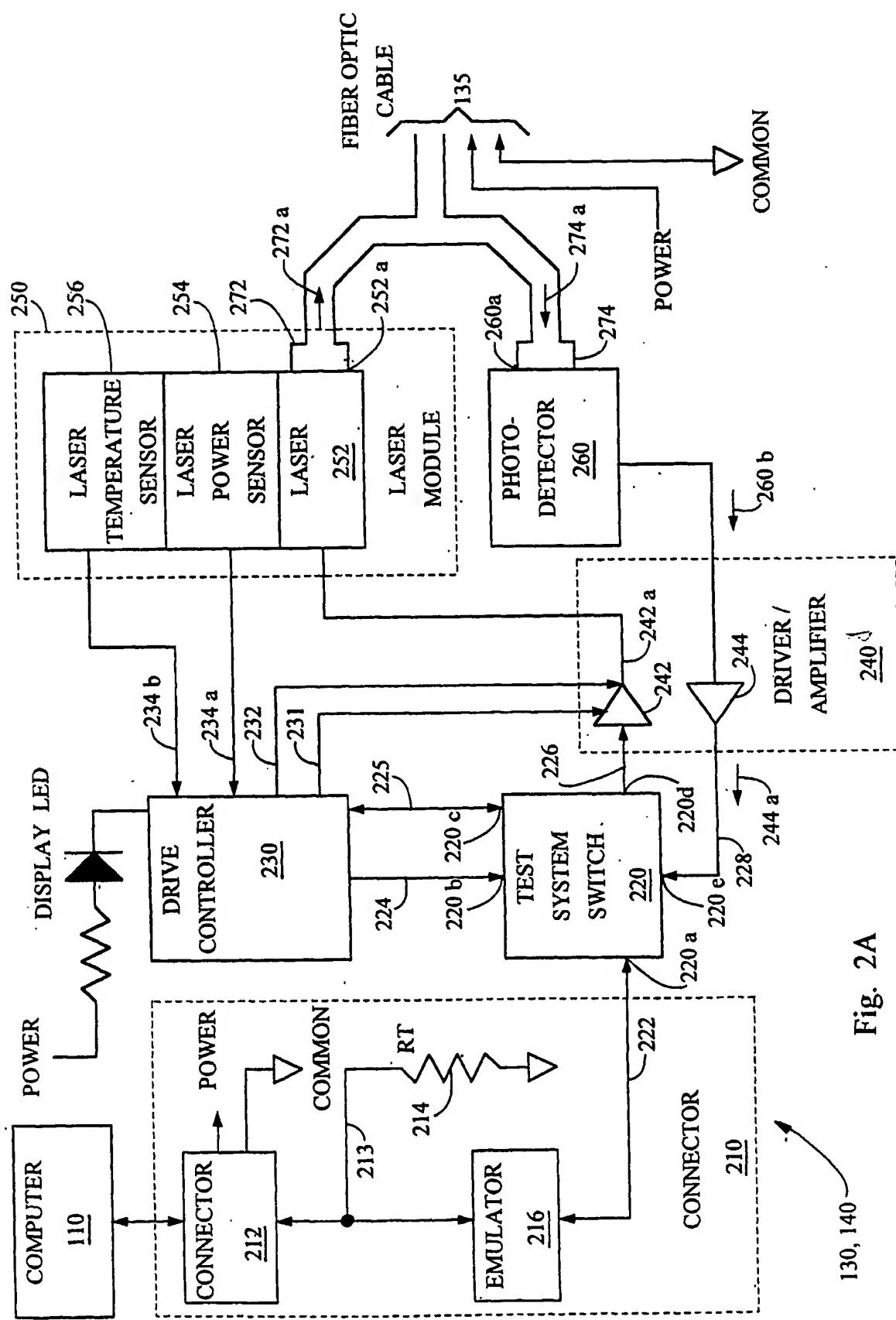


Fig. 1B

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SUBSTITUTE SHEET (RULE 26)

Fig. 2A
130, 140

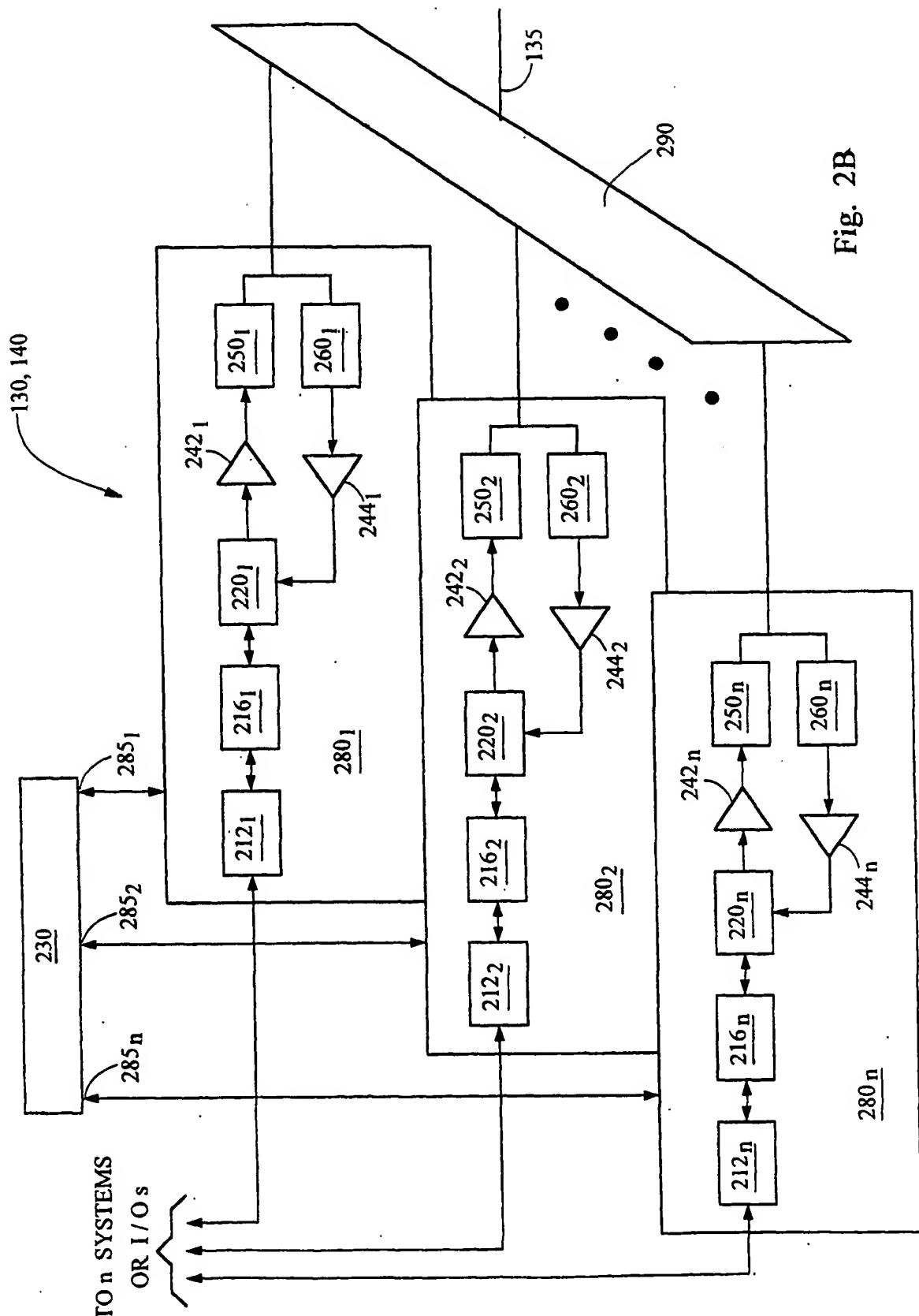


Fig. 2B

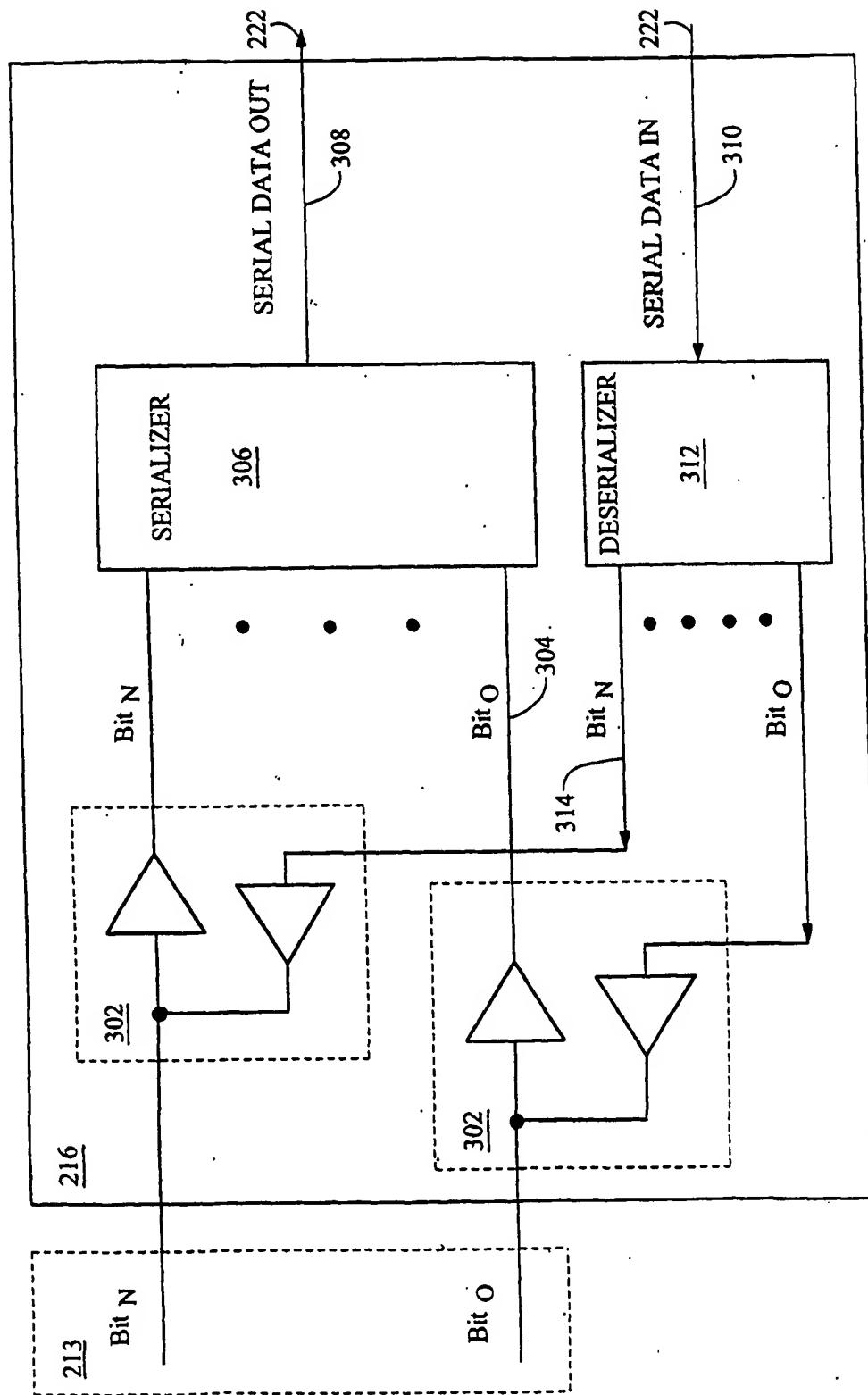


Fig. 3A

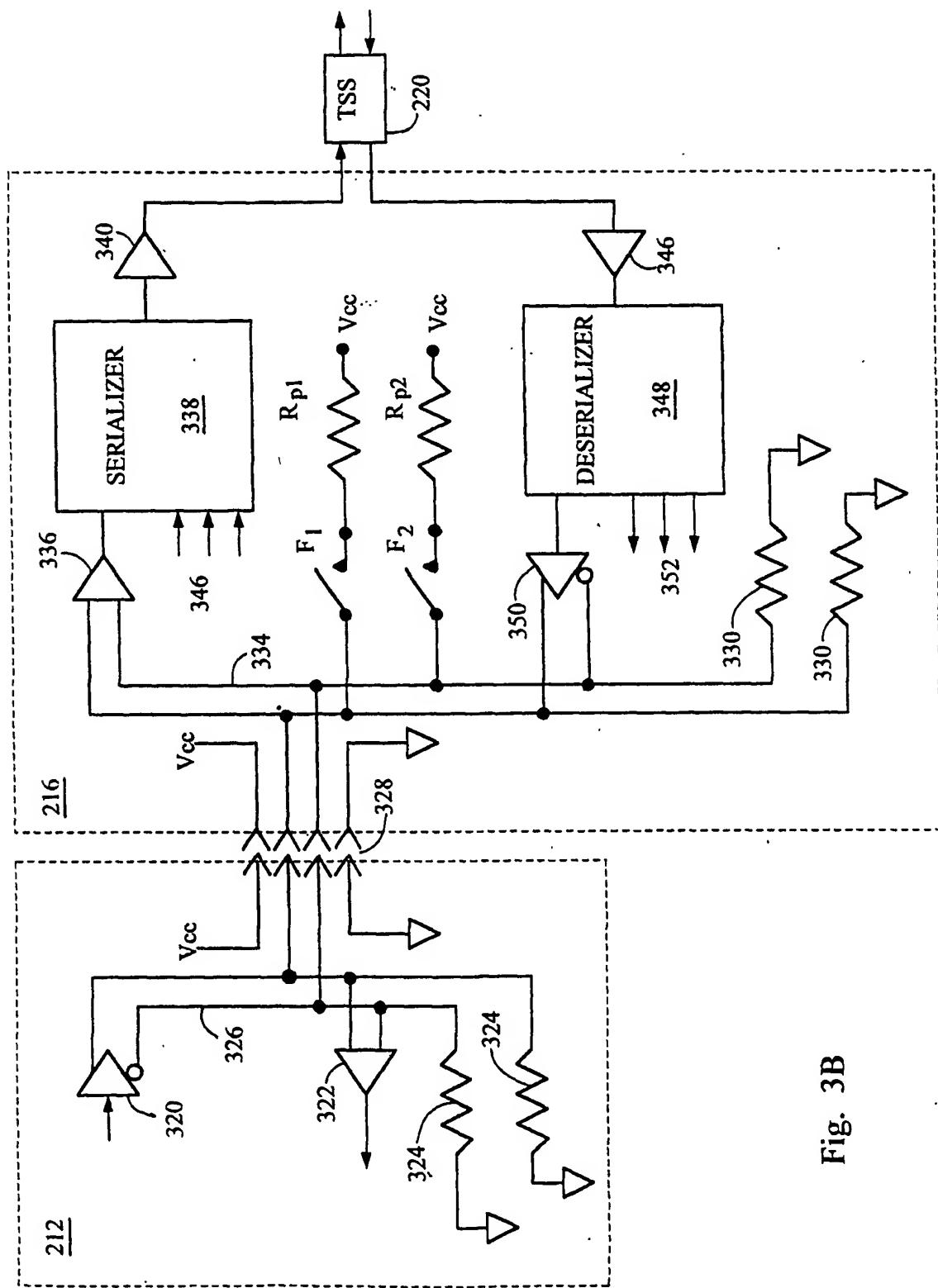


Fig. 3B

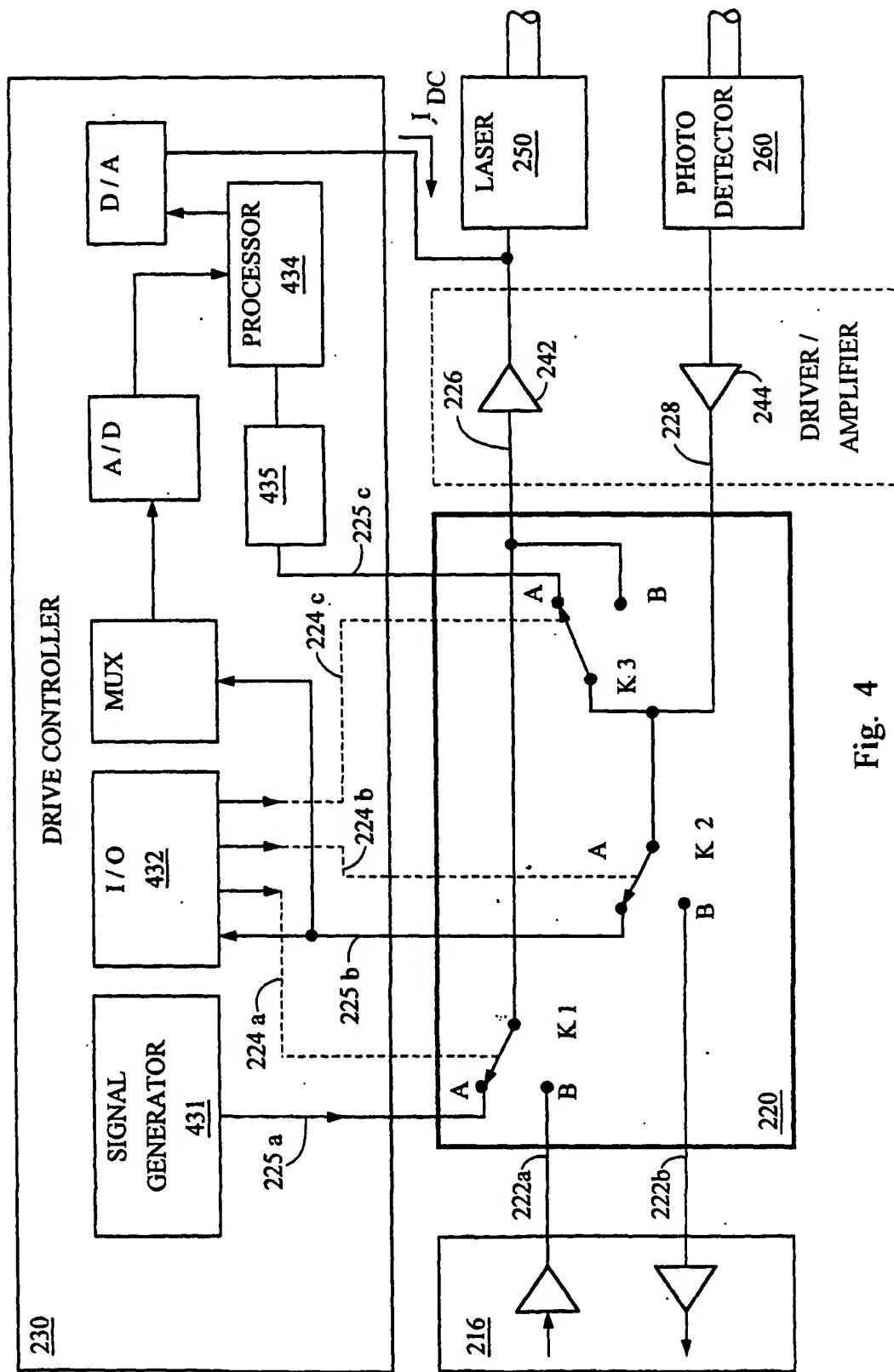


Fig. 4

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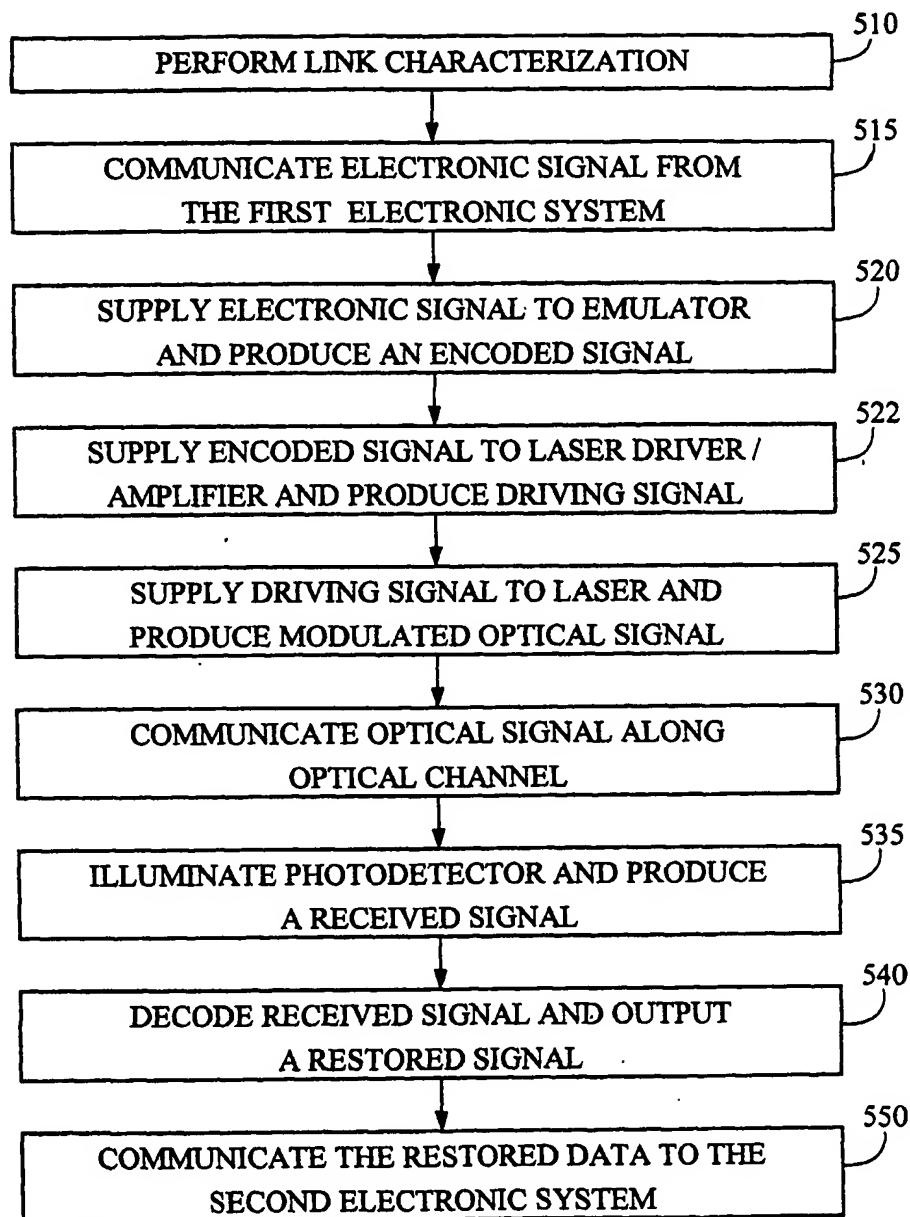


Fig. 5A

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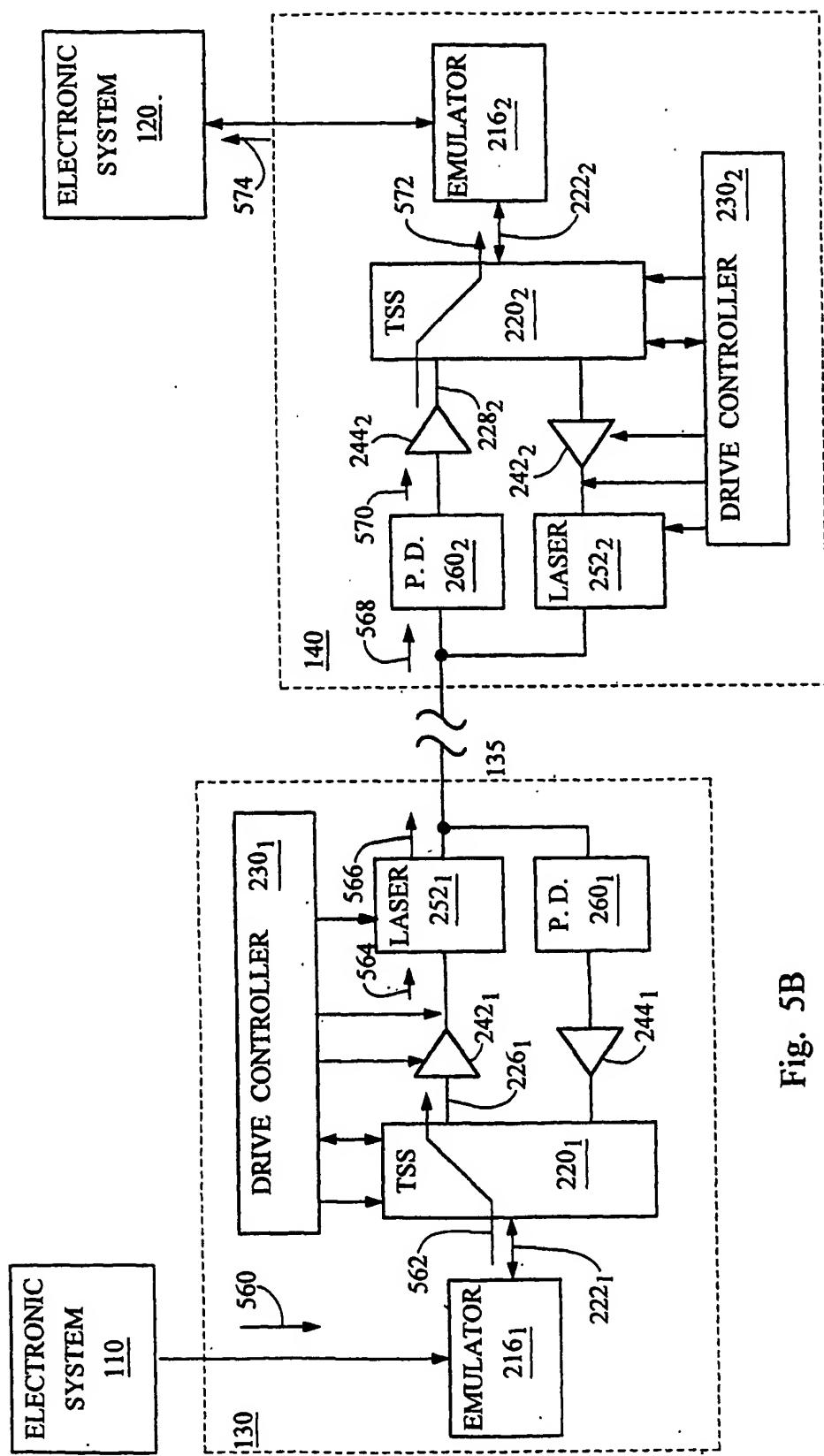


Fig. 5B

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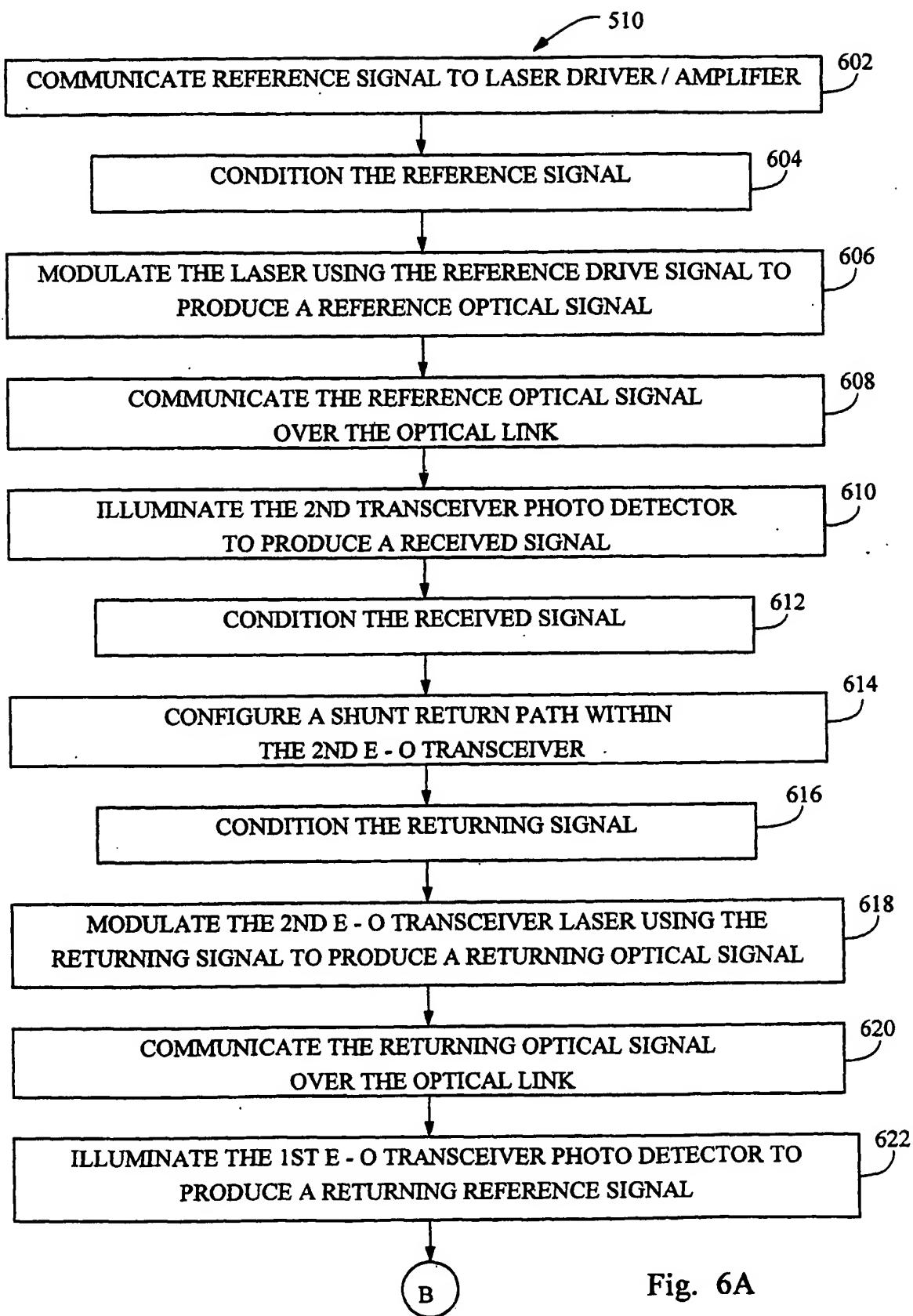


Fig. 6A

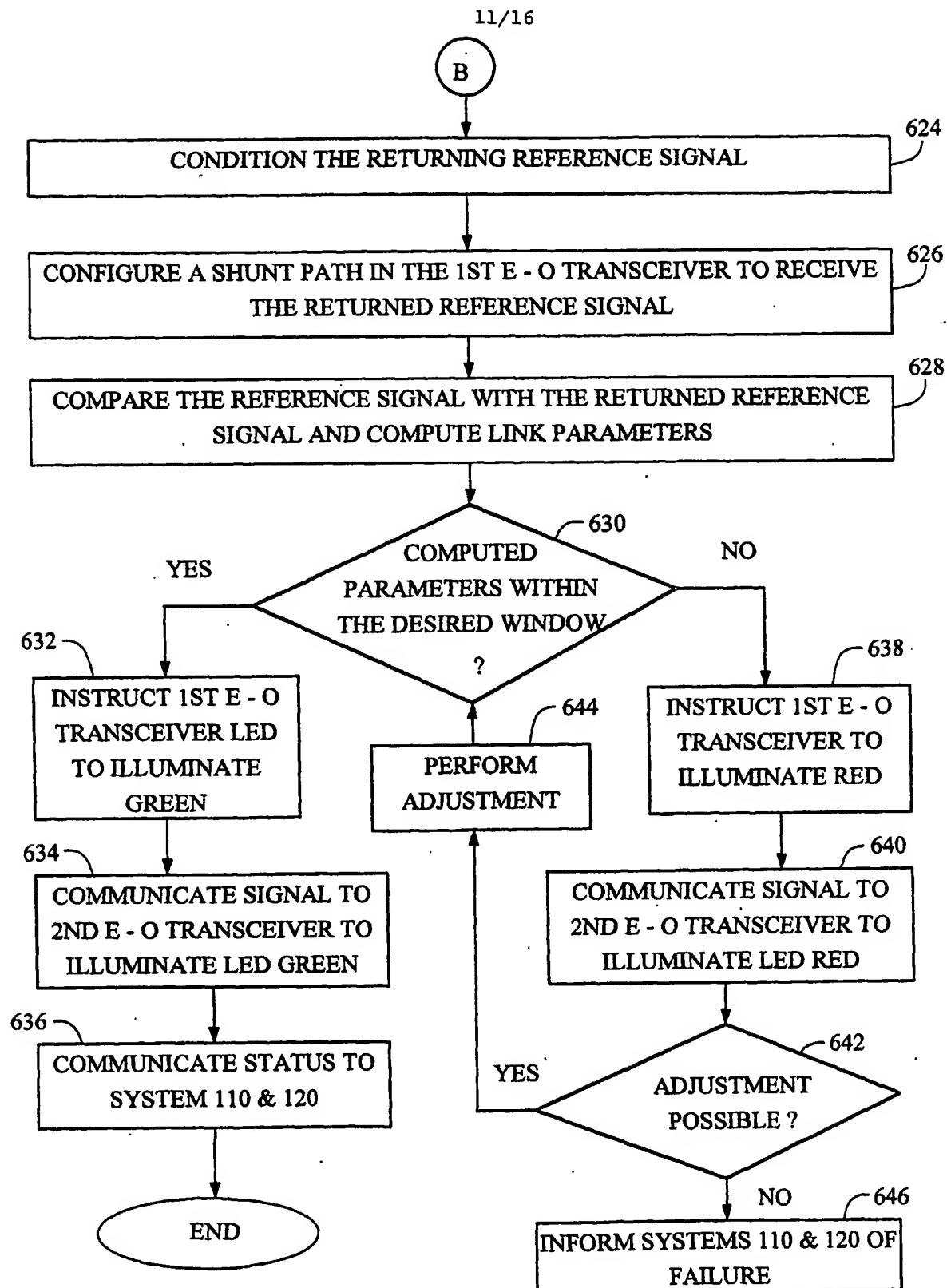


Fig. 6B

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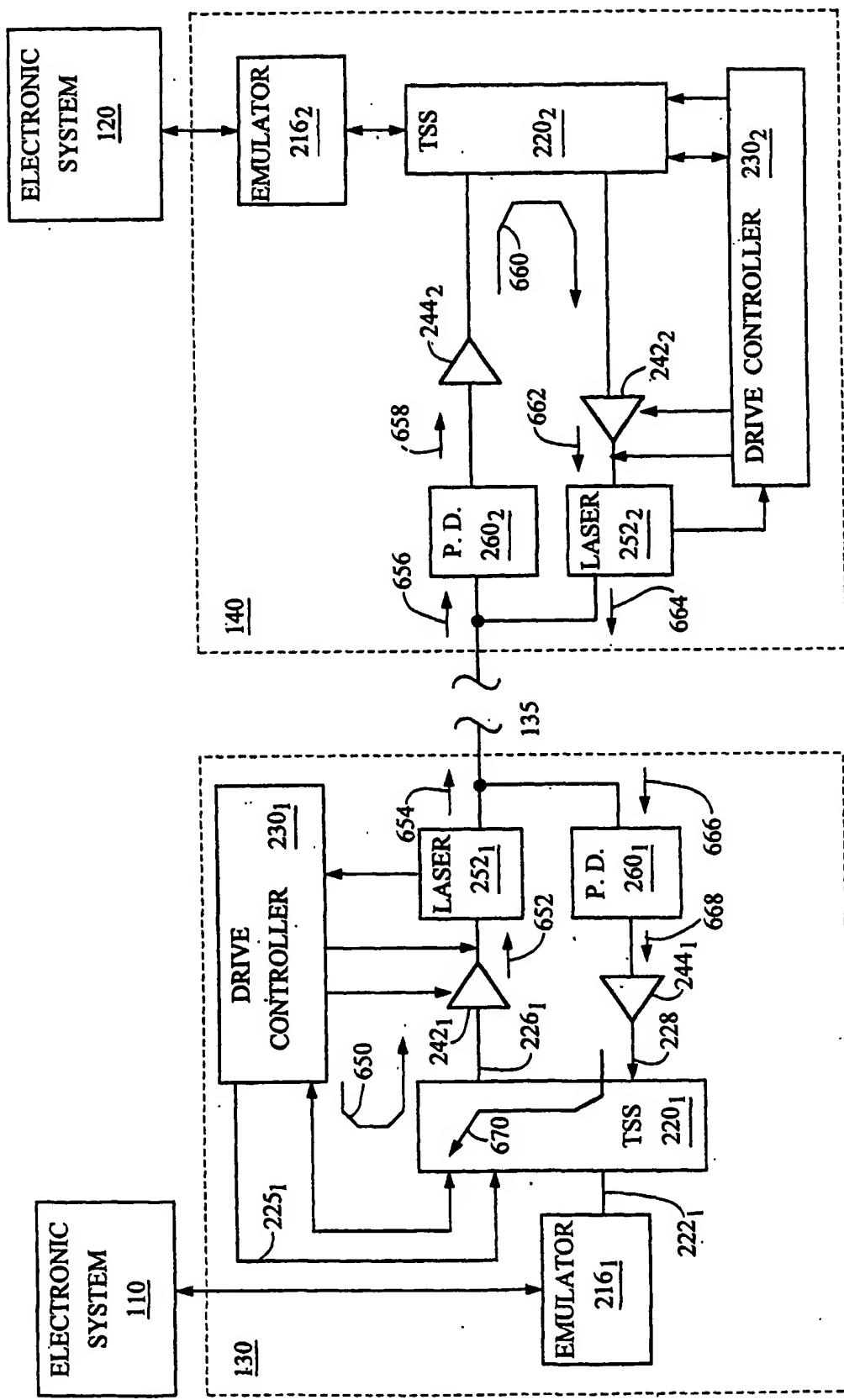


Fig. 6C

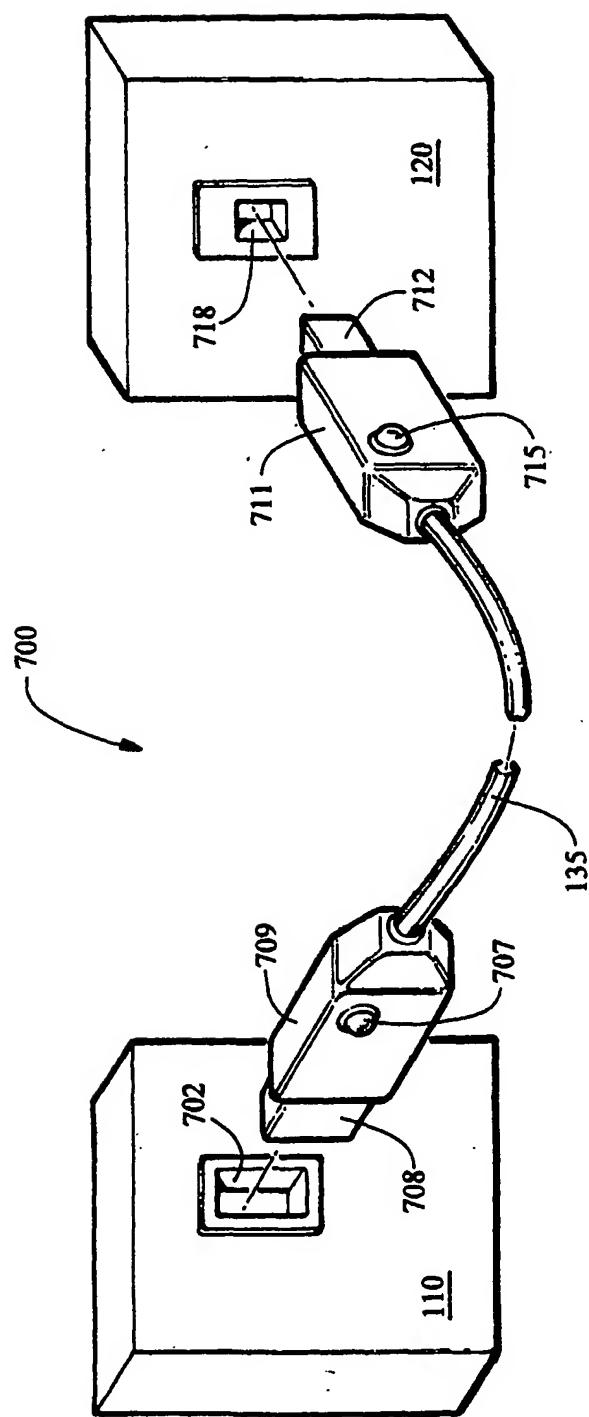


Fig. 7

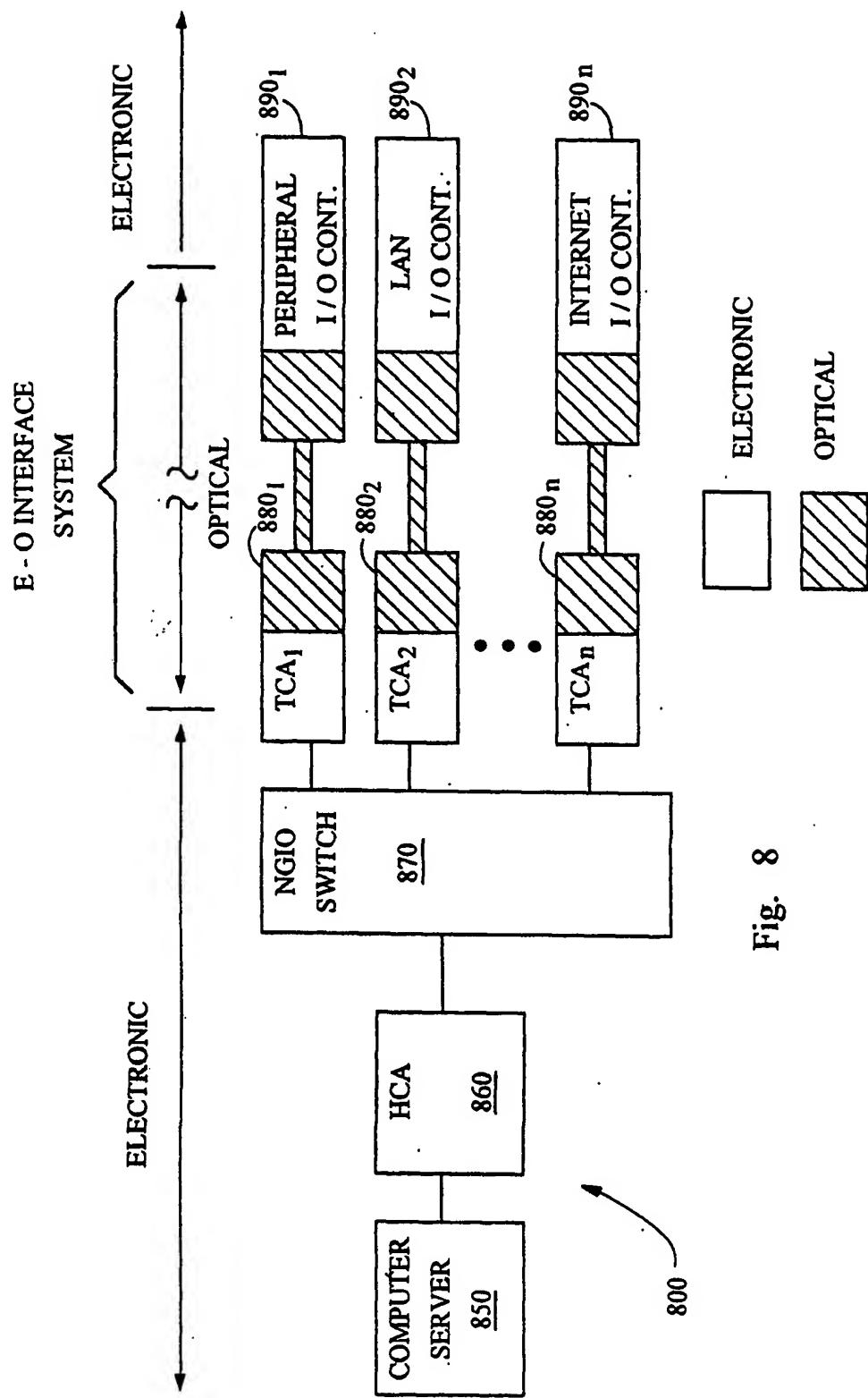


Fig. 8

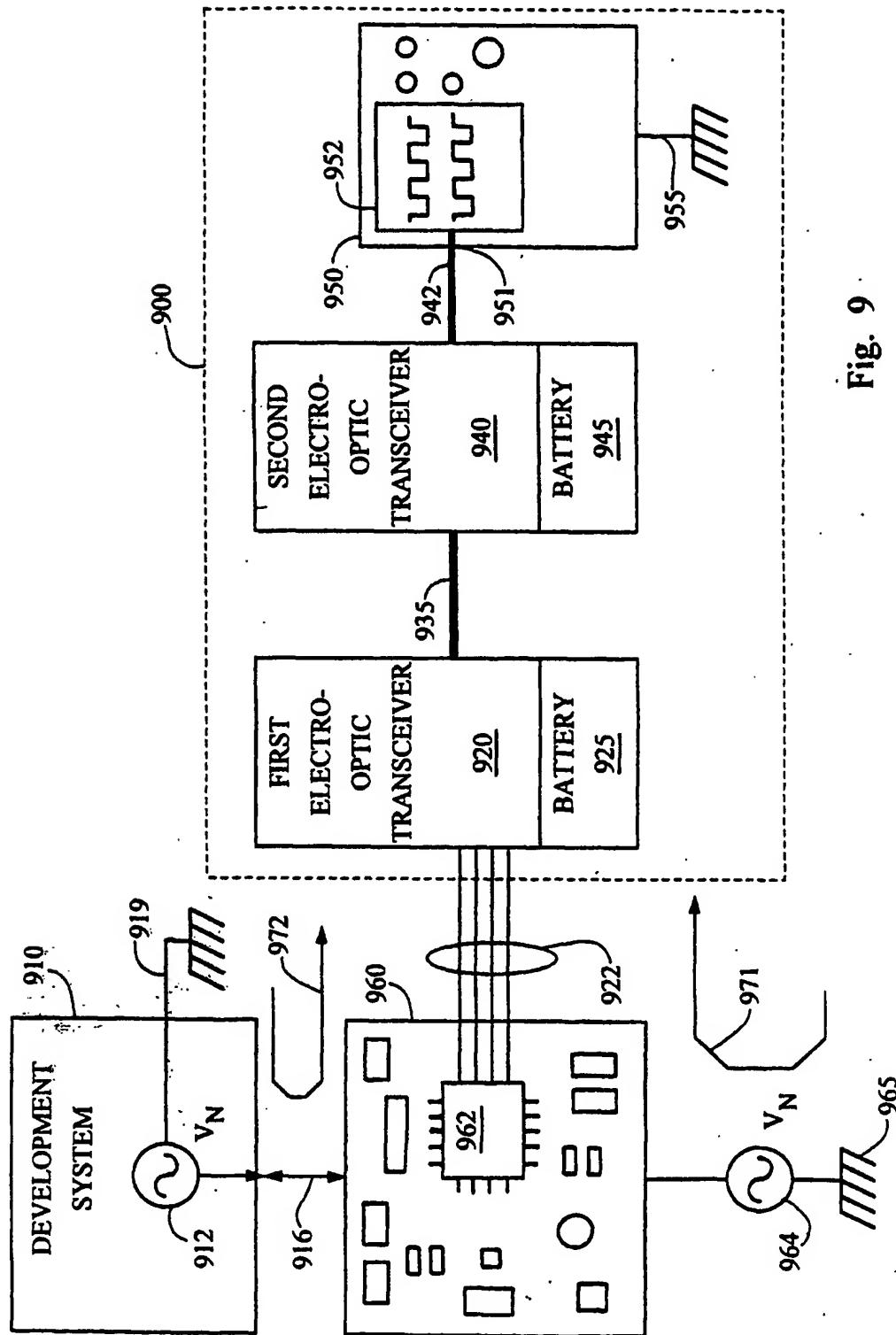


Fig. 9

Table 1
Signal Path for Test System Switch

	Line (s) 222	Line (s) 225	Line (s) 226	Line (s) 228
Line (s) 222		225 ← 222 Local Link Test	226 ← 222 Transmission	222 ← 228 Reception
Line (s) 225	225 ← 222 Local Link Test		226 ← 225 Link Test	225 ← 228 Link Test
Line (s) 226	226 ← 222 Transmission	226 ← 225 Link Test		226 ← 228 Link Test
Line (s) 228	222 ← 228 Reception	225 ← 228 Link Test	226 ← 228 Link Test	

Fig. 10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/35123A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B10/152

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 759 666 A (FUJITSU LTD) 26 February 1997 (1997-02-26)	14,15, 19-23
A	column 5, line 25 -column 6, line 44; claim 1; figures 2-4	1-3, 8-11,13, 16,24
Y	---	14,15, 19-23
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 040 (E-159), 17 February 1983 (1983-02-17) & JP 57 190436 A (FUJI DENKI SEIZO KK;OTHERS: 01), 24 November 1982 (1982-11-24) abstract	1
	---	-/-

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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- *O* document referring to an oral disclosure, use, exhibition or other means
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T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the International search

Date of mailing of the International search report

26 March 2001

03/04/2001

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Authorized officer

Goudelis, M

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/35123

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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JP 61012138 A	20-01-1986	NONE		